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Charge Domain Folding ADC for Multi-bit ΔΣ AD Modulator

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Abstract. This paper describes consideration on folding ADC usage inside a multi-bit ΔΣ AD modulator. The folding ADC requires only one comparator for each bit with analog preprocessing circuits; hence, it requires only small hardware and its power consumption is small for 5-bit or 6-bit resolution. Further its latency is small (one or two clock cycles) compared to an SAR ADC or a pipelined ADC. We propose to use a 5-bit or 6-bit ADC and a 3-bit DAC inside the modulator. We consider that thanks to these characteristics, 5-bit or 6-bit ΔΣ AD modulator can be implemented using the folding ADC. Also, our designed charge mode folding ADC employing discrete-time signal processing in Gray code output format is shown with SPICE simulation results using TSMC 0.18μm CMOS SPICE parameters. It may suffer from nonlinearity due to device mismatches, but it will be noise-shaped inside the modulator and its effects will be alleviated.

1. Introduction

A multi-bit ΔΣ AD modulator is attractive because the quantization noise of the ADC inside is reduced and the multi-bit DAC improves the high-order modulator loop stability as well as the integrator operational amplifier swing is reduced. Also, in a continuous-time modulator, the DAC clock jitter effects are alleviated. The multi-bit ADC inside the modulator improves the signal-to-[quantization noise + distortion] ratio (SQNDR) by 3 dB for 1-bit resolution increase [1]. In many cases, the resolution of the ADC inside the modulator is limited up-to 3-bit or at most 4-bit when the flash-type ADC architecture is employed. The 3-bit flash ADC uses 7 comparators while the 4-bit one uses 15 comparators. For the 5-bit flash one, 31 comparators are required and for the 6-bit one, 63 comparators are needed; these require relatively large hardware and consume a lot of power. When an SAR ADC is employed inside the modulator, high resolution can be realized with small hardware and power. However, its latency is long, which degrades the output rate of the modulator.

In this paper, usage of the folding ADC inside the multi-bit ΔΣ AD modulator is investigated; even in the 6-bit resolution case, only 6 comparators with some analog encoding circuits are required and

its latency is only one or two clock cycles. Also, extension of the Leslie-Singh ΔΣ modulator architecture [2, 3] is shown, which can employ e. g., a 6-bit folding ADC and a 3-bit DAC inside the modulator. In the 2nd or 3rd order modulator, a 3-bit DAC may be enough in many cases; more than 3-bit resolution DAC requires extra hardware and power without much benefits to the modulator. Further, as an example of the 5-bit folding ADC, the charge mode one is shown with its simulation results.

Our charge domain folding ADC uses switches and capacitors, which are suitable for CMOS implementation, and its preliminary ideas are shown in [4, 5]. There are other folding ADCs which uses switched capacitors [6, 7], but our folding ADC is different from them mainly because ours uses saturation or sigmoid characteristics of the pre-amplifier. Previously current domain folding ADC was developed for bipolar transistor implementation, because the bipolar transistor has good current driving capability [8], however recently its CMOS implementations as well as its design methodologies have been reported [9-21]. The advantages of our charge domain folding ADC are that there is very few additional hardware to realize analog encoding very fast without high frequency signal generation internally.

2.1 Extension of Leslie-Singh Architecture

Leslie and Singh proposed a second-order ΔΣ AD modulator in [2] which uses a multi-bit ADC and a single-bit DAC (Fig. 1), which can reduce the quantization noise of the ADC inside the modulator and avoid the nonlinearity of the DAC; it is because the single-bit DAC is inherently linear whereas the multi-bit DAC has some nonlinearities. However, the single-bit DAC usage sacrifices the advantages of the multi-bit DAC usage; the loop stability improvement and the integrator operational amplifier swing reduction, as well as the DAC jitter effect reduction in a continuous-time modulator.

Hence, we investigate a ΔΣ AD modulator which uses a 6-bit or 5-bit folding ADC and a 3-bit DAC with the data-weighted-averaging (DWA) algorithm logic, with the same structure as the Leslie-Singh architecture (Fig.2). The upper 3 bits of the 6-bit or 5-bit folding ADC are applied to the inputs of the 3-bit DAC with Data-Weighted Averaging (DWA) logic. This investigated structure would be well-balanced; the usage of a 6-bit DAC may lead to too much hardware and power with only small performance improvement, and the 3-bit DAC would suffice. Also see [32] in the 1st-order modulator case.

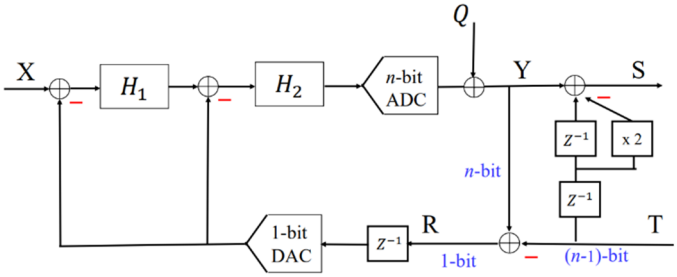


Fig. 1. Leslie-Singh 2nd-order ΔΣ AD modulator with an *n*-bit ADC and a 1-bit DAC.

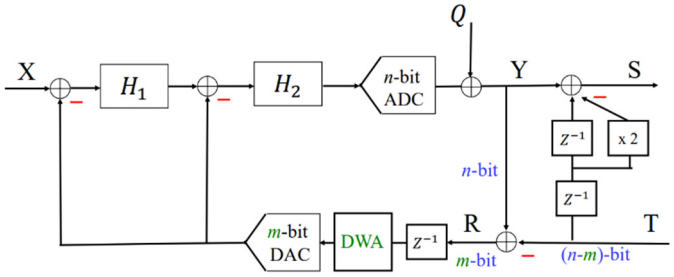


Fig. 2. Investigated 2nd-order ΔΣ AD modulator with an *n*-bit ADC and an *m*-bit DAC (*n*>*m*).

In Figs. 1 and 2, we have the following:

$$[1 + Z^{-1}H_2(Z)\,[1 + H_1(Z)]]\,Y(Z)$$
$$= Q(Z) + H_2(Z)H_1(Z)X(Z) + Z^{-1}H_2(Z)\,[1 + H_1(Z)]T(Z) \quad (1)$$

Here, $X(Z)$ is the input signal, $Y(Z)$ is the n-bit ADC output, Q(Z) is the ADC quantization noise, and $S(Z)$ is the modulator output. Here we consider the second-order modulator, and hence $H_1(Z)$ and $H_2(Z)$ are analog integrators, given by

$$H_1(Z) = \frac{1}{1-Z^{-1}}\ ,\quad H_2(Z) = \frac{1}{1-Z^{-1}}. \quad (2)$$

T(Z) is the lower (*n*-*m*) bits of the *n*-bit ADC output, while R(Z) the upper *m* bits of the *n*-bit ADC output. In Fig. 1, *m*=1, and in Fig. 2, we consider *n*=5 or 6 and *m*=3. In other words, the internal *m*-bit DAC is driven by the upper m-bit of the *n*-bit ADC output. Then we have the followings:

$$Y(Z) = X(Z) + (1 - Z^{-1})^2\ Q(Z) + (-Z^{-2} + 2Z^{-1})T(Z) \quad (3)$$

By simple digital calculation, we have the modulator output:

$$S(Z) = Y(Z) + (-2\,Z^{-1} + Z^{-2})T(Z) = X(Z) + (1 - Z^{-1})^2 Q(Z) \quad (4)$$

We see that the quantization noise $Q(Z)$ is the second-order noise-shaped. Notice that S(Z) can be obtained from calculation of the ADC output Y(Z) and its lower (n-m)-bits T(Z) in a feedforward manner as shown in Eq. (4), it is not included in Eq. (1).

Note that the DWA logic in Fig. 2 is for the noise-shaping of the multi-bit (*m*-bit, *m*>1) nonlinearities [1, 33].

2.2 Charge Mode Folding ADC

We describe here our charge mode folding ADC design with TSMC 0.18μm CMOS SPICE parameters and 3V supply voltage. Its circuit and SPICE simulation results are shown in this subsection. We have designed a 6-bit folding ADC but due to space limitation, only a 5-bit case is shown. The resolution of 6-bit can be easily realized with simple hardware.

Its digital output is provided in Gray code format (Table 1, Fig. 3), and the Gray code can be converted to the binary code using exclusive OR (EXOR) gates; the 2-input EXOR gate can be realized with 2 PMOSFETs and 2 NMOSFETs [34].

The preamplifier circuit and its SPICE simulation results are shown in Fig. 4. Preamplifier saturation characteristics is used and nonlinear switched capacitor folding circuit can be designed. In the preamplifier, the parameter of transistors as following: $(W/L)_{input}$=2μm/0.2μm, $(W/L)_{p1}$=1.5μm/0.2μm, $(W/L)_{p2}$=2μm/0.2μm and the tail current is 50μA. We simulated the delay time of the preamplifier with load capacitance changes when current is 50μA (Fig. 4 (c)), and tail current changes with 0.03pF load capacitance (Fig. 4 (d)). In the condition of 0.03pF load capacitance with 50μA, the preamplifier has a 0.95ns delay time. Here the load capacitance is the one between Vout+ and ground and the one between Vout- and ground in Fig. 4 (a).

The circuit configurations, operations and SPICE simulation results for G4, G3, G2, G1, G0 generation are shown in Figs. 5, 6, 7, 8 and 9, respectively, where transient simulations were performed for the ramp input Vin. In phase 1, the output of each preamplifier is sampled and stored in each capacitor. In phase 2, the preamplifier output and the capacitor are disconnected. Then each capacitor is connected. Notice that the differential capacitor outputs are connected alternately (Fig. 10). Its analog encoding is done in charge domain and discrete-time, which is suitable for CMOS implementation. In

other words, analog encoding is done by just connection, and hence it reduces hardware and power significantly compared to the flash ADC.

This can avoid CMOS low current drivability. Its conversion latency is one or two-clock, which is comparable to the flash ADC. If this ADC is used stand alone, it may suffer from device mismatches such as preamplifier and comparator offsets, which lead to the whole ΔΣ ADC nonlinearity. However, it is used inside the modulator, the nonlinearity is noise-shaped and does not affect the whole modulator linearity significantly (Fig. 10).

Also notice that in phase 1 the preamplifier tail current can be cut off for power reduction.

Table 1. Binary code and Gray code

Decimal number	Binary Code	Gray Code
0	00000	00000
1	00001	00001
2	00010	00011
3	00011	00010
4	00100	00110
5	00101	00111
6	00110	00101
7	00111	00100
8	01000	01100
9	01001	01101
10	01010	01111
11	01011	01110
12	01100	01010
13	01101	01011
14	01110	01001
15	01111	01000

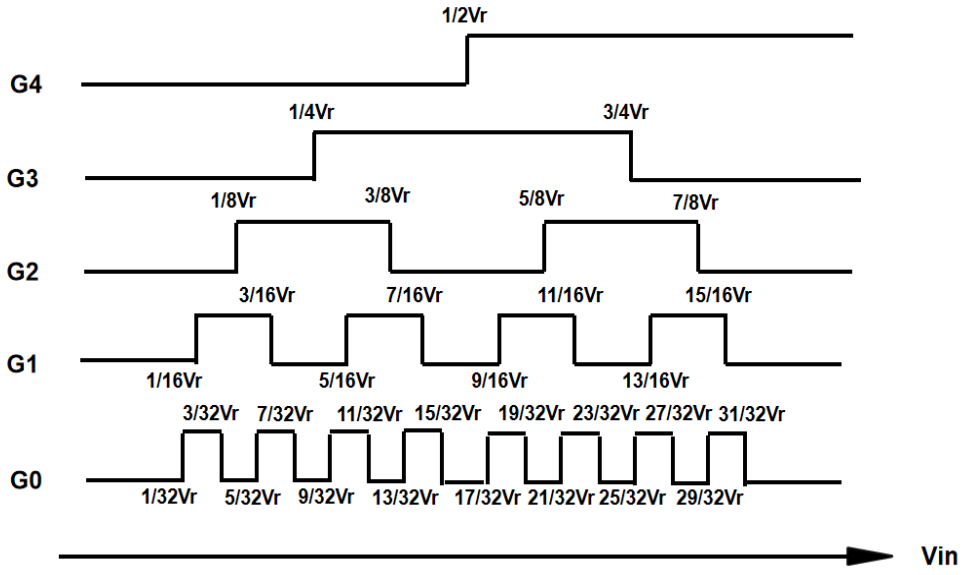
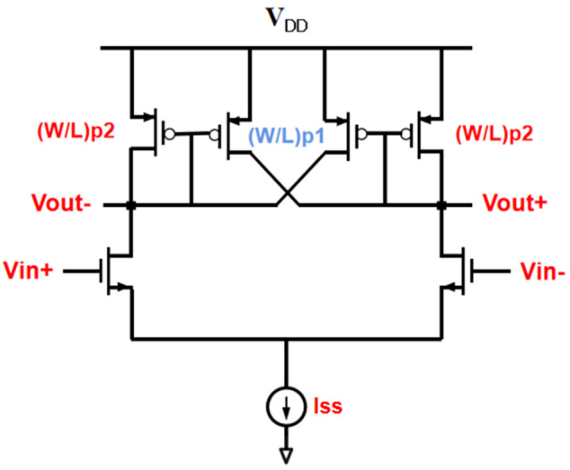
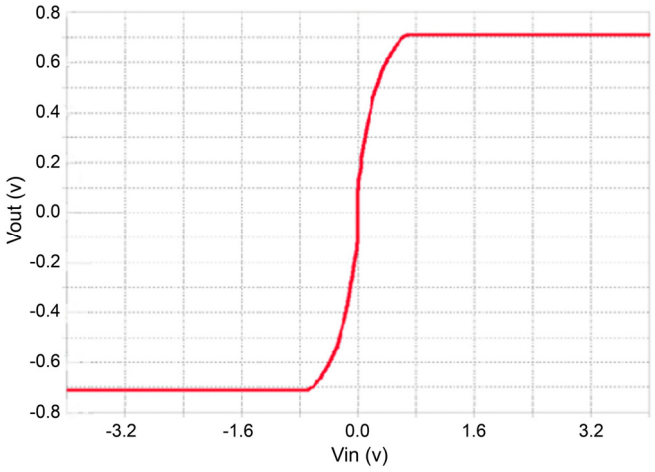


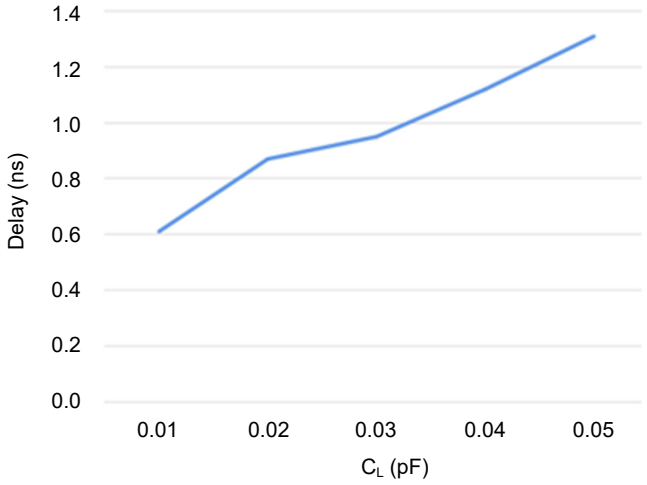
Fig. 3. Gray code digital output with respect to the analog input Vin.



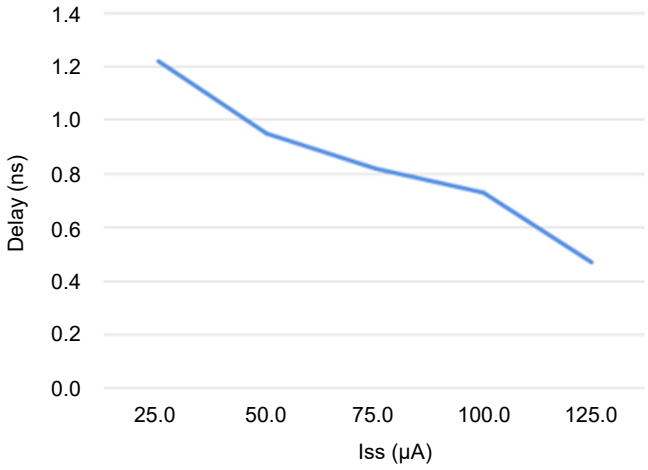
(a) Circuit configuration



(b) SPICE simulation results (ΔVout /ΔVin)

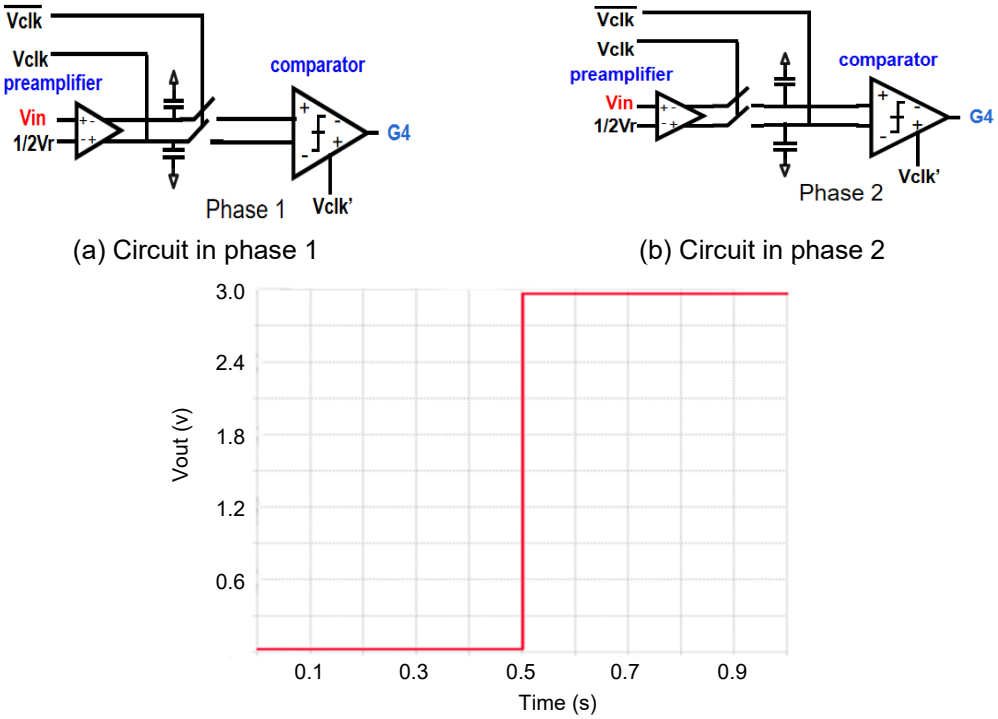


(c) Simulation results of delay time with load capacitance changes, where the tail current is 50 μA



(d) Simulation results of delay time with tail current changes, where the load capacitance is 0.03 pF

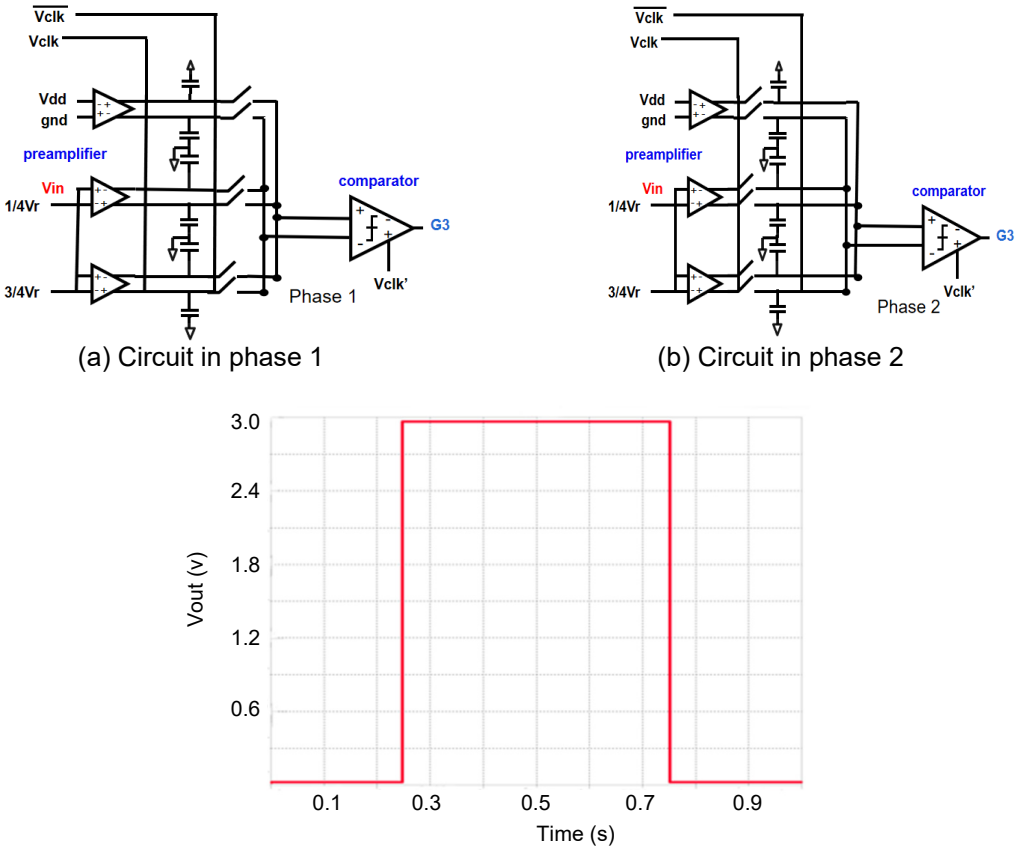
Fig. 4. Pre-amplifier circuit.



(a) Circuit in phase 1 (b) Circuit in phase 2

(c) SPICE transient simulation result for the ramp input

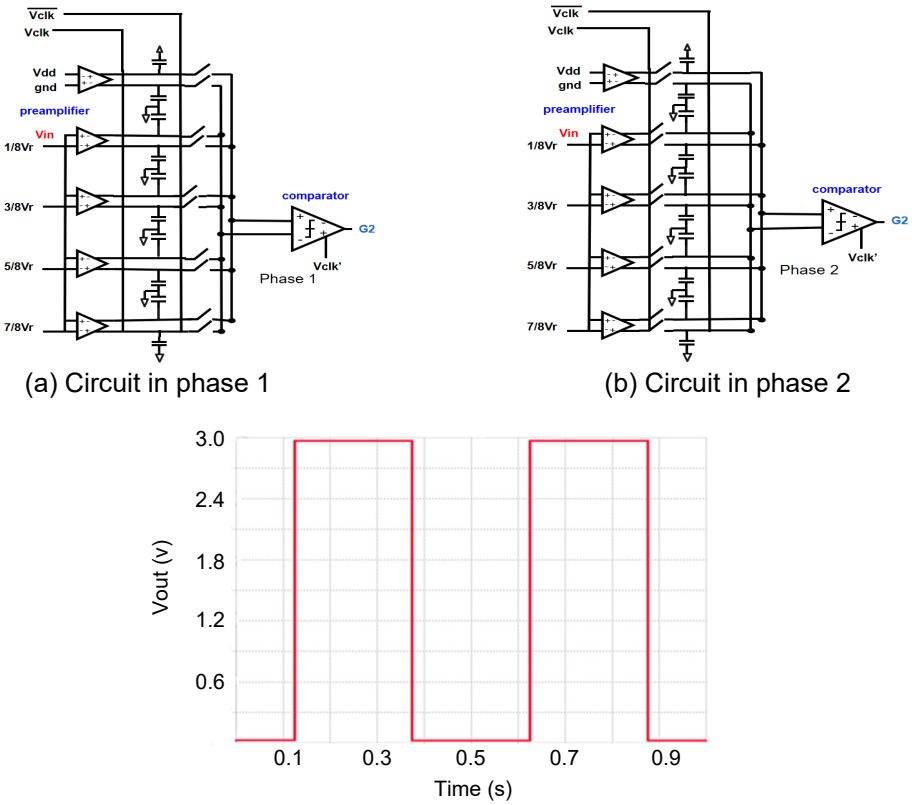
Fig. 5. MSB (G4) generation circuit of the proposed charge-domain folding ADC.



(a) Circuit in phase 1 (b) Circuit in phase 2

(c) SPICE transient simulation result for the ramp input

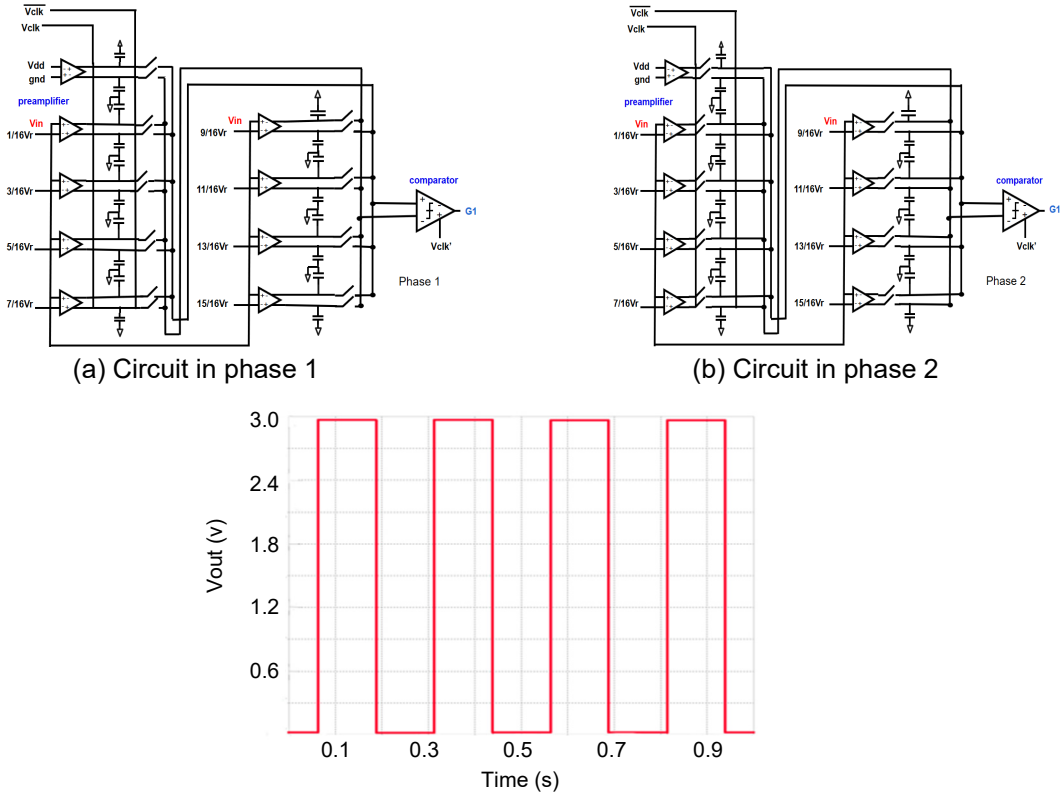
Fig. 6. MSB-1 (G3) generation circuit of the proposed charge-domain folding ADC.



(a) Circuit in phase 1 (b) Circuit in phase 2

(c) SPICE transient simulation result for the ramp input

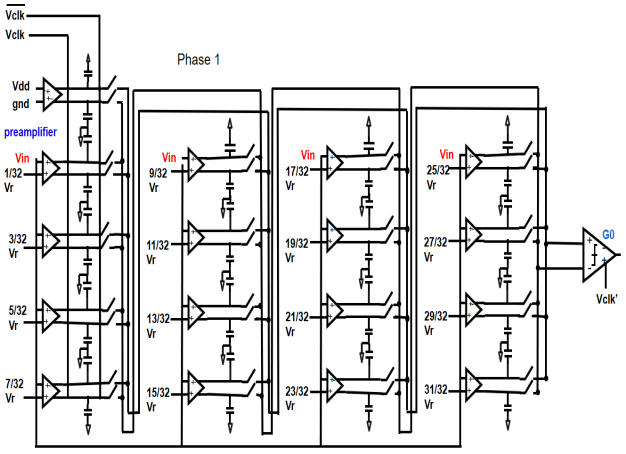
Fig. 7. MSB-2 (G2) generation circuit of the proposed charge-domain folding ADC.



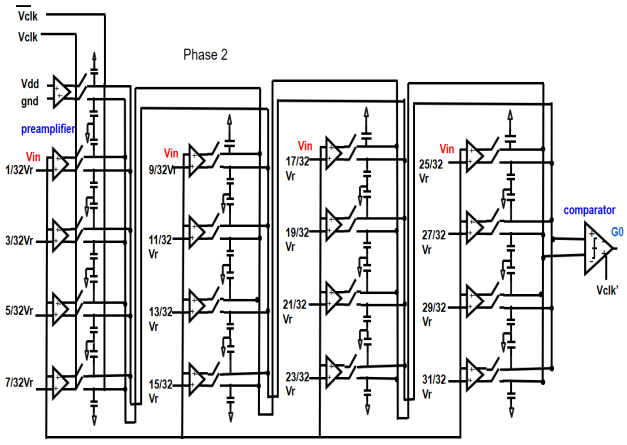
(a) Circuit in phase 1 (b) Circuit in phase 2

(c) SPICE transient simulation result for the ramp input

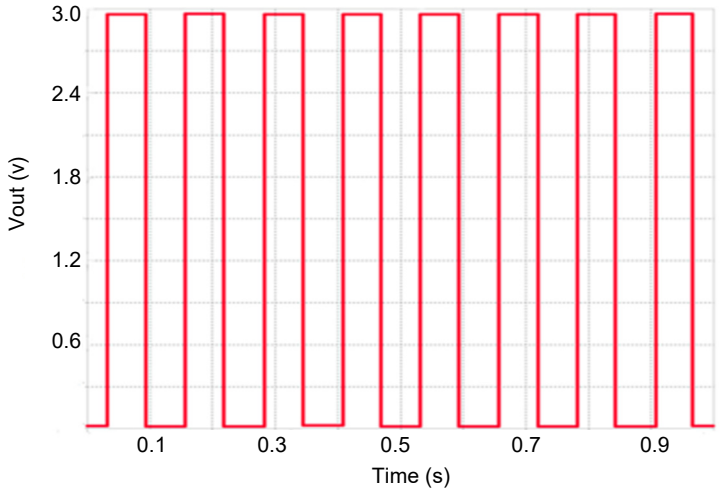
Fig. 8. MSB-3 (G1) generation circuit of the proposed charge-domain folding ADC.



(a) Circuit in phase 1

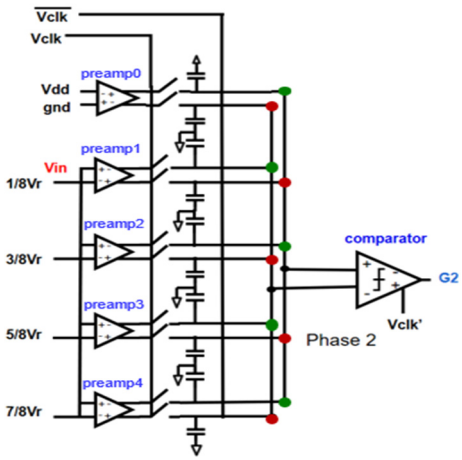


(b) Circuit in phase 2

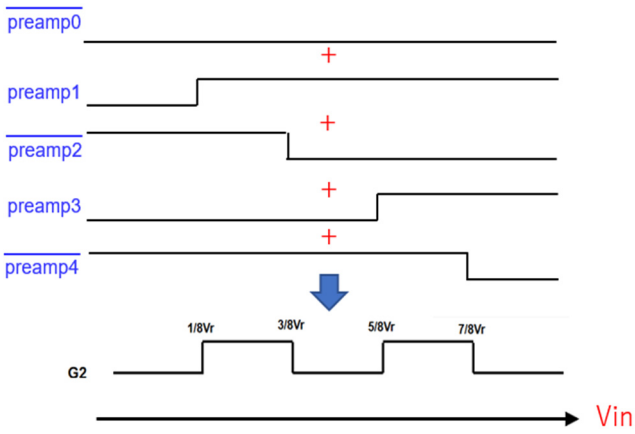


(c) SPICE transient simulation result for the ramp input

Fig. 9. LSB (G0) generation circuit of the proposed charge-domain folding ADC.



(a) G2 generation circuit



(b) Its output generation explanation

Fig. 10. Explanation of analog encoding for G2 generation.

3. Conclusion

In this paper, usage of the folding ADC inside the multi-bit ΔΣ AD modulator is investigated; the 6-bit resolution ADC inside the modulator can be realized with small latency and small circuitry as well low power. Also, extension of the Leslie-Singh architecture is shown, which employs a 6-bit folding ADC and a 3-bit DAC with DWA inside the modulator. Finally, we remark that the folding ADC can be also used inside the pipelined ADC with the similar arguments as the contents described in this paper.

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