Journal of Technology and Social Science (JTSS)

High Reliability and Low Switching Loss Dual RESURF 40 V N-LDMOS Transistor with Grounded Multi-Step Field Plate

Jun-ichi Matsuda[a,*], Anna Kuwana[b], and Haruo Kobayashi[c]

Division of Electronics and Informatics, Gunma University, 1-5-1, Tenjin-cho Kiryu, Gunma, 376-8515, Japan

*Corresponding author

[a]<jun-ichi.matsuda@nifty.com>, [b]<kuwana.anna@gunma-u.ac.jp>, [c]<koba@gunma-u.ac.jp>

Keywords: LDMOS, reliability, switching loss, grounded field plate, step field plate

Abstract. This paper proposes a high reliability and low switching loss dual RESURF 0.18 μm CMOS compatible process 40 V N-LDMOS transistor with a grounded multi-step (two or three-step) field plate, used as integrated switching devices of power supplies for automotive applications. Device simulation verified that the electric field along the interface near the gate-side drift region edge for the two-step and the three-step devices is 67 % and 46 % of a conventional LDMOS transistor with a flat field plate connecting to the gate, respectively. This result indicates that the proposed devices have much higher hot carrier endurance and a large SOA by suppressing the current expansion at a high drain current. The power FOM deteriorates in the order of the conventional device, the two-step device, and the three-step device, but the difference in the FOM is very slight. The switching loss of the proposed device is about 50 % of the conventional one. The proposed device is suitable for automotive applications used in harsh environments. We can choose the two or three-step structure depending on the required specification and the process cost.

1. Introduction

Low power output and high efficiency switching power supplies for automotive applications always require LDMOS (Lateral Double Diffused Metal Oxide Semiconductor) transistors with high reliability, large SOA (Safe Operating Area), low specific on-resistance, and low switching loss. To obtain high reliability (or high hot carrier endurance) and large SOA, we proposed a 40 V operation dual RESURF (Reduced Surface Field) LDMOS transistor for the first time [1]. Next, to obtain low specific on-resistance adding to high reliability and large SOA, we improved the LDMOS transistor by connecting a field plate to the gate [2], enhancing the RESURF. Further, to obtain low switching loss by suppressing the Miller effect, the field plate was grounded [3,4,5] and optimized [6]. However, automotive applications operating in harsh environments require much higher hot carrier endurance. Therefore, we have further improved the LDMOS transistor by making the field plate multi-step to reduce the electric field around the gate-side drift region edge, leading to much higher hot carrier endurance.

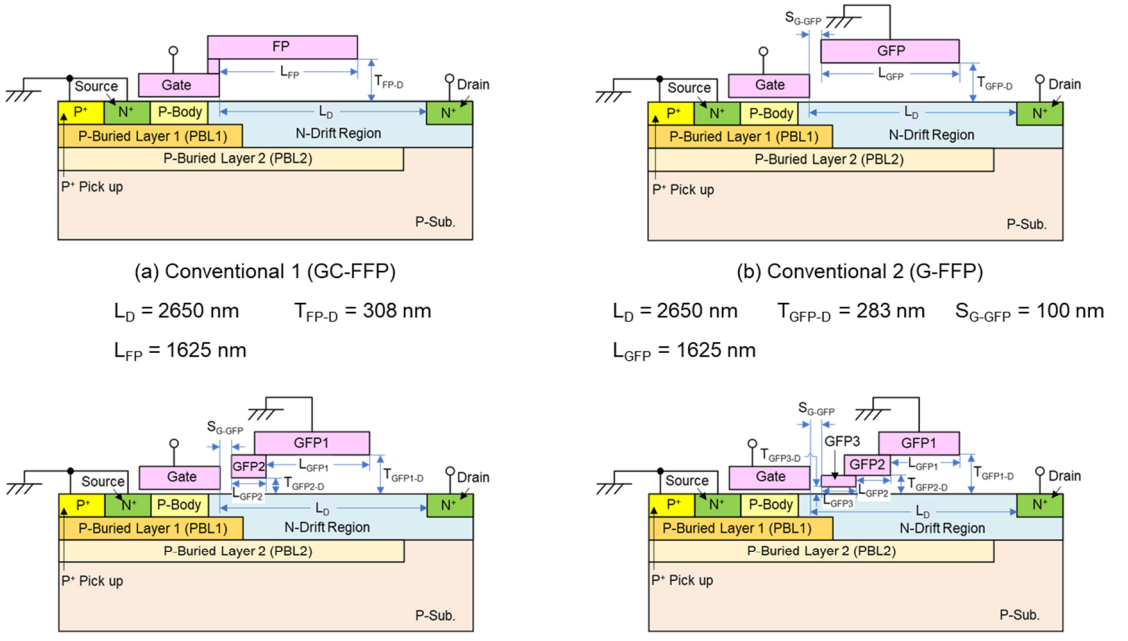
In this paper, we analyze the electrical characteristics of the improved LDMOS transistor with a grounded multi-step field plate: hot carrier endurance, SOA (or drain current expansion) [7], specific on-resistance (R_{ON_SP}) vs. drain-to-source breakdown voltage at the off-state (BV_{DS_OFF}), and switching loss, using the device simulator in 3D TCAD developed by AdvanceSoft Corporation [8].

2. Device Structures and Process Flow

Fig.1 shows rough cross-sectional views of the conventional and the proposed LDMOS transistors. Fig. 1 (a) shows a conventional LDMOS transistor with the gate connected to a flat field plate (Conventional 1: GC-FFP), (b) a conventional LDMOS transistor with a grounded flat field plate (Conventional 2: G-FFP), (c) a proposed LDMOS transistor with a grounded two-step field plate

(Proposed 1: G-2FP), and (d) a proposed LDMOS transistor with a grounded three-step field plate (Proposed 2: G-3FP). A 0.18 μm CMOS compatible process can make these devices. Here G-FFP optimizes the field plate formation with a space of 100 nm between the field plate and the gate based on [5] to compare with the proposed devices needing the space. The lengths of the field plates of GC-FFP, G-FFP, G-2FP, and G-3FP are the same. The proposed devices have a strong RESURF around the gate-side drift region compared to the conventional ones due to the multi-step field plate. The lower field plate in G-2FP, GFP2, is optimally designed to obtain as much uniform electric field in the drift region upon drain-to-source breakdown at the off-state as possible. The oxide thickness between the lowest field plate in G-3FP, GFP3, and the drift region is thinner than that between GFP2 in G-2FP and the drift region to get a much higher RESURF effect. The middle field plate in G-3FP, GFP2, is optimally designed to obtain as much uniform electric field in the drift region upon drain-to-source breakdown at the off-state as possible.

Fig. 2 shows a rough cross-sectional view of the impurity regions in the substrate of G-FFP, whose profile is the same as those of other devices. Table 1 shows net impurity doses along cut lines in Fig. 2. These impurity doses are optimized to obtain an adequate power FOM (Figure of Merit: $BV_{DS\_OFF}^2/R_{ON\_SP}$) for GC-FFP. Two P-type buried layers, PBL1 and PBL2, for those devices form a dual RESURF structure which reduces the electric field in the drift region adequately. Three N-type drift layers, NDL1, NDL2, and NDL3, form the N-drift region. NDL1 is the base layer of the N-drift region, NDL2 enhances N-type impurity concentration in the surface region to reduce CE (drain current expansion), and NDL3 compensates for the increase in the N-drift resistance due to the grounded field plate, and also reduces CE. The extrapolated threshold voltage, V_T, is 1.05 V for all the devices.



(a) Conventional 1 (GC-FFP)

L_D = 2650 nm T_{FP-D} = 308 nm

L_{FP} = 1625 nm

(b) Conventional 2 (G-FFP)

L_D = 2650 nm T_{GFP-D} = 283 nm S_{G-GFP} = 100 nm

L_{GFP} = 1625 nm

(c) Proposed 1 (G-2FP)

L_D = 2650 nm T_{GFP1-D} = 283 nm S_{G-GFP} = 100 nm

L_{GFP1} = 1225 nm T_{GFP2-D} = 108 nm

L_{GFP2} = 400 nm (L_{GFP1} + L_{GFP2} = 1625 nm)

(d) Proposed 2 (G-3FP)

L_D = 2650 nm T_{GFP1-D} = 283 nm S_{G-GFP} = 100 nm

L_{GFP1} = 725 nm T_{GFP2-D} = 148 nm

L_{GFP2} = 500 nm T_{GFP3-D} = 58 nm

L_{GFP3} = 400 nm (L_{GFP1} + L_{GFP2} + L_{GFP3} = 1625 nm)

Fig. 1. Rough cross-sectional views of the conventional and the proposed devices.

Table 1 Net Impurity doses along cut lines in Fig. 2.

Layer	Net Dose [cm^{-2}]		
	A-A'	B-B'	C-C'
NDL	3.17×10^{12}	4.32×10^{12}	4.44×10^{12}
PBL	1.23×10^{13}	1.52×10^{12}	–

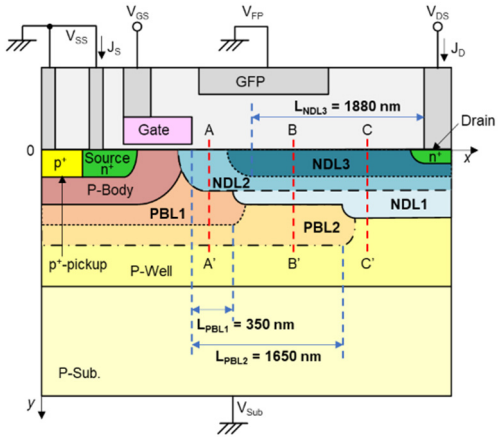


Fig. 2. Rough cross-sectional view of impurity regions in the substrate (G-FFP).

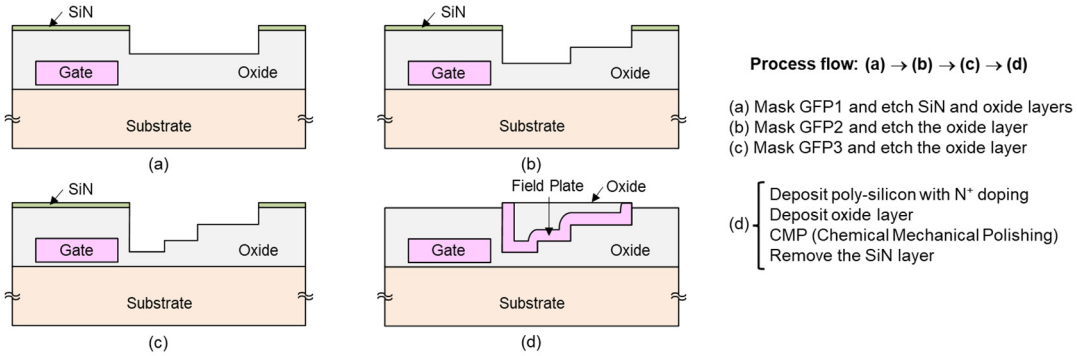


Fig. 3. Rough process flow making the field plate of G-3FP.

Fig. 3 shows a process flow example making the field plate of G-3FP. The cross-section of the field plate in Fig. 3 is not the same as that in Fig. 1, but the RESURF effect between them is the same. The input capacitance in Fig. 3 is higher than that in Fig. 1, but the difference is very slight. SiN makes CMP stop. G-2FP has no (c) process in Fig.3 (one masking and one oxide etching process), decreasing the process cost.

3. Simulation

The electrical characteristics obtained from the device simulator used in this study have an error of less than 5 % compared to those of actual submicron devices [9]. Impurities in the substrate have the Gaussian profile in the vertical direction. The ratio of the lateral to the vertical profile of the impurities in the substrate is 0.7.

Fig. 4 shows the circuit simulating switching (turn-on and turn-off) characteristics. The supply voltage to the drain, V_{D_Supply}, and the gate, V_{G_Supply}, is 40 V and 3.3 V, respectively. The resistance of the load R_L and the gate R_G is 1.06 Ωmm^2 and 5.33 Ωmm^2, respectively, for an LDMOS transistor layout area of 1 mm^2.

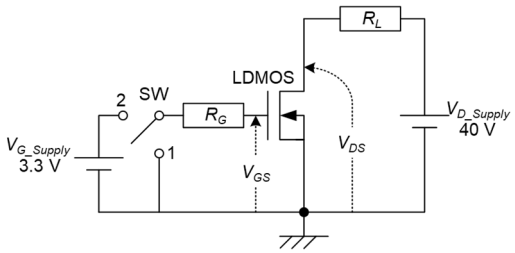


Fig. 4. Circuit simulating switching characteristics. R_G = 1.06 Ωmm^2 and R_L = 5.33 Ωmm^2 are used for an LDMOS transistor layout area of 1 mm^2.

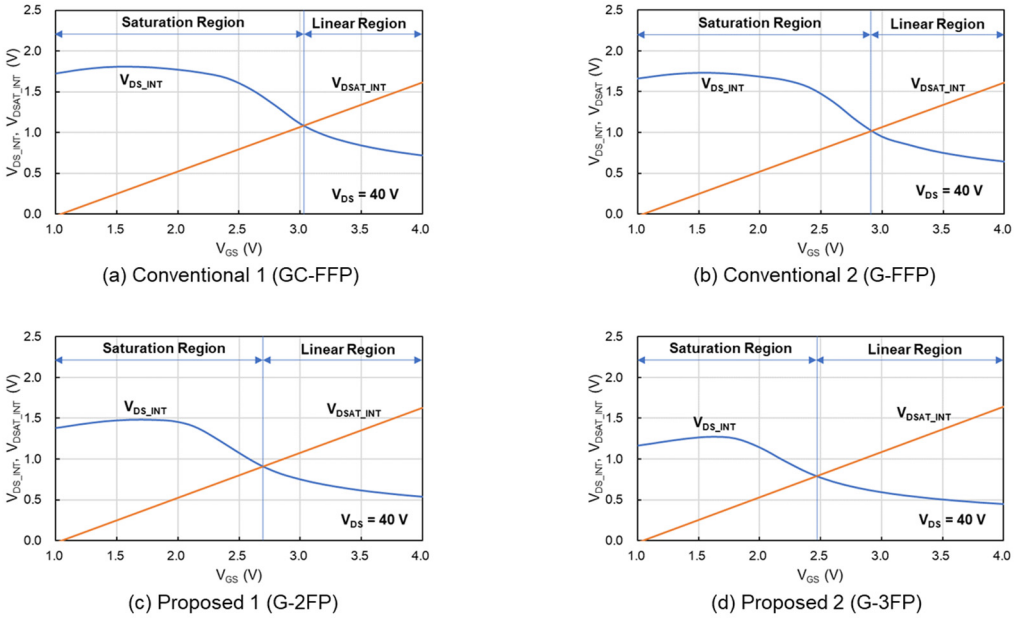
4. Results and Discussion

4.1 Hot Carrier Endurance

Fig. 5 shows the dependence of the gate-source voltage, V_{GS}, on the drain voltage of the intrinsic MOSFET, V_{DS_INT}, and the saturation voltage of that, V_{DSAT_INT}, for GC-FFP, G-FFP, G-2FP, and G-3FP. V_{DS_INT} is the interface voltage at the drain-side gate edge. The following equation derives V_{DSAT_INT} [10].

$$V_{DSAT\_INT} = (V_{GS} - V_T)/\alpha \tag{1}$$

Here α is a coefficient related to the depletion charge under the channel and can be obtained using the source current vs. V_{DS_INT} characteristics from the device simulation. (See Appendix.) From Fig. 5, we can see the operation region of the intrinsic MOSFET. The saturation region for V_{GS} at a drain-source voltage, V_{DS}, of 40 V becomes narrower in the order of GC-FFP, G-FFP, G-2FP, and G-3FP due to lower V_{DS_INT} caused by stronger RESURF. This result means that the duration of the hot carrier stress under the saturation state during the turn-on and turn-off process is shorter in the same order, and V_{DS_INT} as hot carrier stress voltage is lower in the same order.



(a) Conventional 1 (GC-FFP)

(b) Conventional 2 (G-FFP)

(c) Proposed 1 (G-2FP)

(d) Proposed 2 (G-3FP)

Fig. 5. Dependence of V_{GS} on V_{DS_INT} and V_{DSAT_INT}.

From Fig. 5, the intrinsic MOSFET is in the saturation state under a bias condition of V_{GS} = 2 V and V_{DS} = 40 V for all the devices. Therefore, by taking the bias condition as hot carrier stress, the electric field profiles along the interface in the minus x-direction for GC-FFP, G-FFP, G-2FP, and G-3FP are

shown in Fig. 6. (See Fig. 2 for x-direction.) The electric field around the gate-side drift region edge becomes lower in the order of GC-FFP, G-FFP, G-2FP, and G-3FP. This tendency corresponds to the reduction of V_{DS_INT} aforementioned. The electric field for G-2FP and G-3FP is 67 % and 46 % of GC-FFP, respectively. This result states that G-3FP has the highest hot carrier endurance for the intrinsic MOSFET. Here G-2FP has peak electric fields at the drain-side edge of GFP1 and GFP2, and G-3FP, at the drain-side edge of GFP1, GFP2, and GFP3. Since these peak electric fields are high, they may cause significant impact-ionizations due to the high energy (or hot) electron current. However, since the electron current path is inside the drift region away from the interface, hot electrons causing impact-ionization and hot holes generated by impact-ionization would not affect the interface in the drift region, leading to high hot carrier endurance. (See Fig. 7 for electron current path, and see Fig. 8 for hole current path.) The grounded multi-step field plate causes deeper electron current paths.

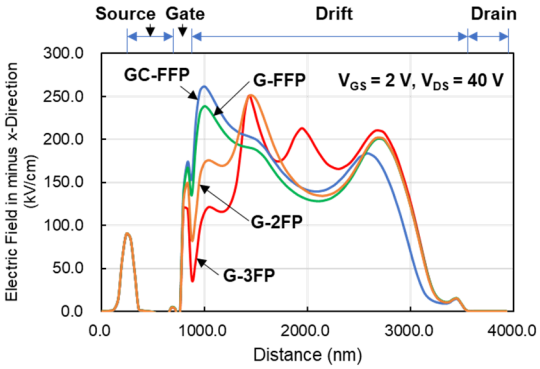


Fig. 6. Electric field profiles in the minus x-direction along the interface depending on device structures under V_{GS} = 2 V and V_{DS} = 40 V.

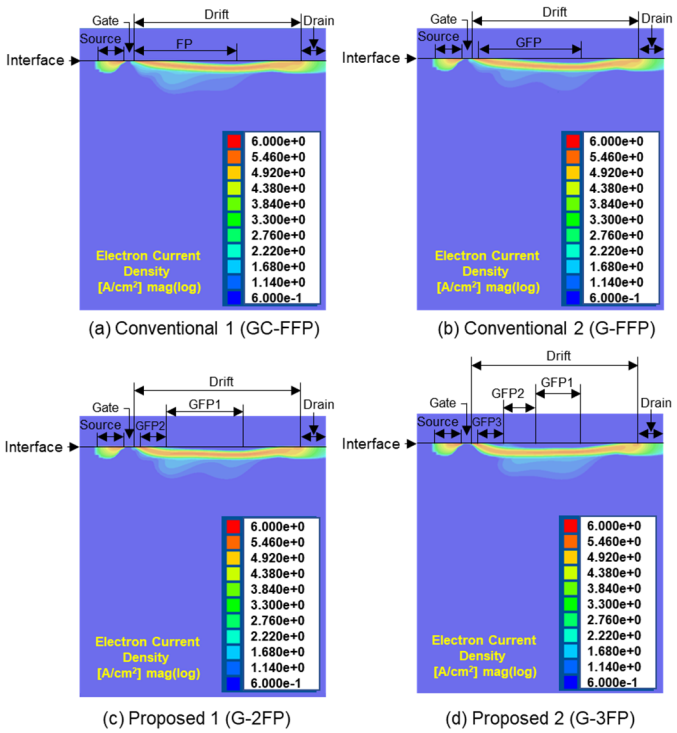


Fig. 7. Electron current density distributions under V_{GS} = 2 V and V_{DS}= 40 V depending on device structures. The electron current path in the drift region for the proposed devices is deeper inside the drift region than that for the conventional devices due to the multi-step field plate.

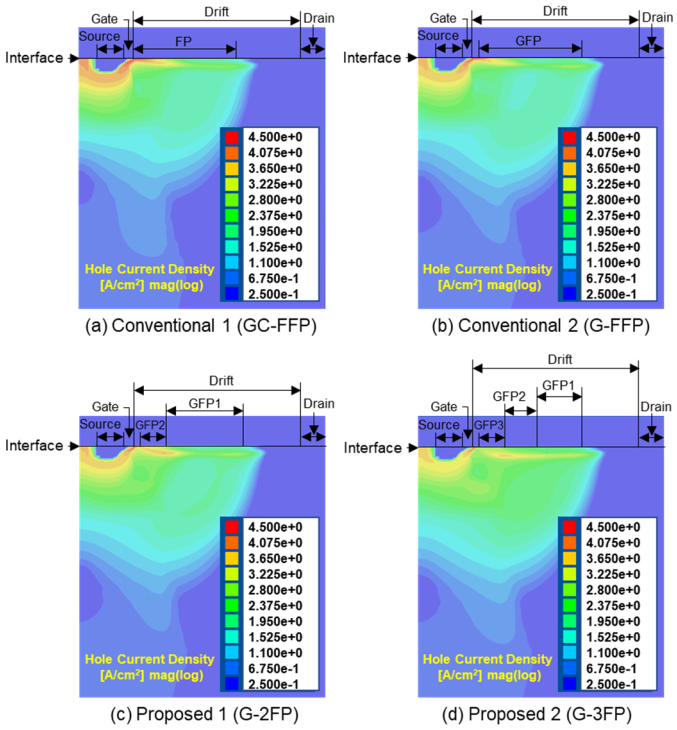


Fig. 8. Hole current density distributions under V_{GS} = 2 V and V_{DS}= 40 V depending on device structures. The proposed devices with the multi-step field plate have lower hole current densities near the gate-side drift region edge than the conventional devices. Also, the hole current density near the drain-side field plate edges for all the devices is higher inside the drift region, away from the interface.

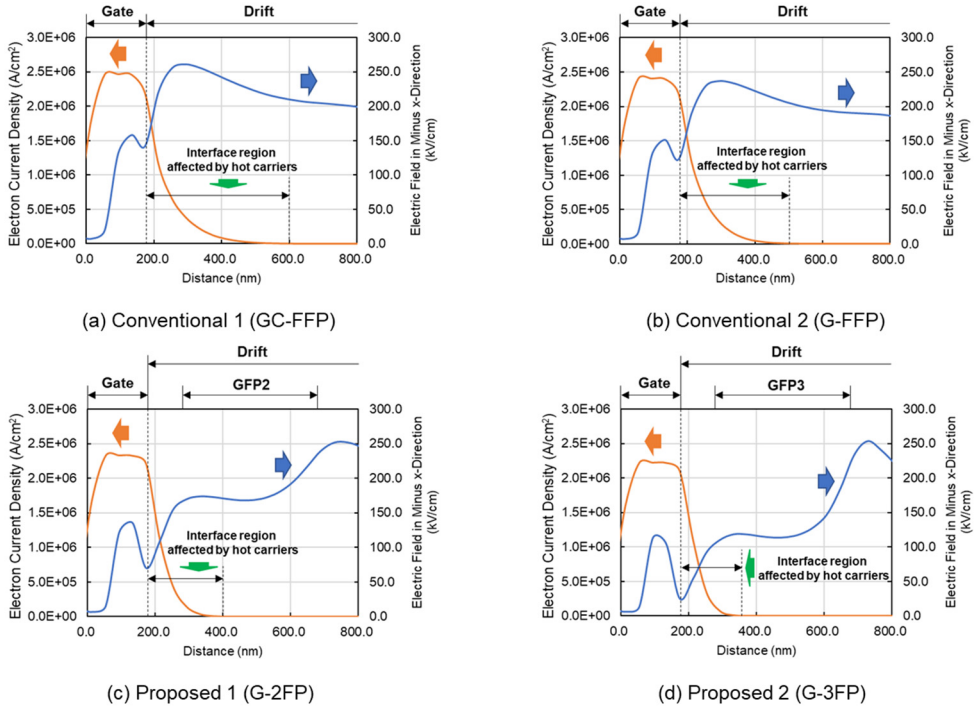


Fig. 9. Electron current density profile and the electric field profile (in the minus x-direction) along the interface at y = 2 nm around the gate-side drift region edge under V_{GS} = 2 V and V_{DS}= 40 V depending on device structures.

Fig. 9 shows the electron current density profile and the electric field profile (in the minus x-direction) along the interface at y = 2 nm for GC-FFP, G-FFP, G-2FP, and G-3FP under V_{GS} = 2 V and V_{DS} = 40 V, where the source-side gate edge is zero of x (distance). (See Fig. 2 for y-direction.) The electron current density steeply decreases with distance from the drain-side gate edge in the order of GC-FFP, G-FFP, G-2FP, and G-3FP due to the electric field in the minus y-direction caused by the field plates. The hot electron current near the interface, accelerated by a high electric field in the minus x-direction, causes impact-ionization and may damage the interface. Therefore, we can define the interface region in the gate-side drift region affected by hot carriers shown in Fig. 9. This interface region decreases in the order of GC-FFP, G-FFP, G-2FP, and G-3FP, leading to higher hot carrier endurance in the same order.

4.2 Current Expansion

Fig. 10 shows the characteristics of the drain current density, J_D, vs. V_{DS} for GC-FFP, G-FFP, G-2FP, and G-3FP under V_{GS} = 4 V, whose gate voltage is the maximum rating and prone to cause CE due to a high drain current. Here, we define the breakdown voltage of on-state (or CE generation voltage), BV_{DS_ON}, as V_{DS} at J_D = 100 A/mm^2 for convenience. BV_{DS_ON} for GC-FFP, G-FFP, G-2FP, and G-3FP is 45.4 V, 45.8 V, 49.0 V, and 51.1 V, respectively. The BV_{DS_ON} of the proposed device is higher than those of the conventional device because of the multi-step field plate. The multi-step field plate enhances RESURF near the gate-side drift region edge especially causing the reduction of V_{DS_INT} for the proposed device. (See Fig. 5.) With this reduction, the J_D (or the minus source current density $-J_S$) decreases because the intrinsic MOSFET operates in the linear region under V_{GS} = 4 V and V_{DS} less than roughly 55 V for all the devices. (See Fig. 5 and Appendix for the linear operation and Fig. 2 for the definition of J_S.) Since the decreased J_D suppresses space charge modulation (or Kirk effect) in the drift region [11], the BV_{DS_ON} rises in the abovementioned order.

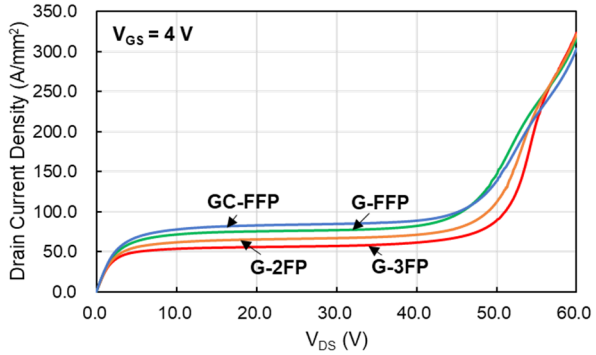


Fig. 10. Drain current density vs. V_{DS} characteristics depending on device structures.

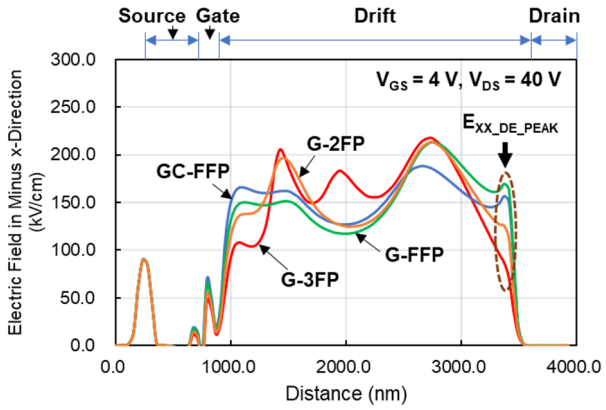


Fig. 11. Electric field profiles in the minus x-direction along the interface depending on device structures under V_{GS} = 4 V and V_{DS} = 40 V.

Fig. 11 shows the electric field profiles in the minus x-direction along the interface under V_{GS} = 4 V and V_{DS} = 40 V for GC-FFP, G-FFP, G-2FP, and G-3FP. GC-FFP and G-FFP have a peak of the electric field near the drain-side drift region edge ($E_{XX\_DE\_PEAK}$) caused by the Kirk effect, respectively. However, the $E_{XX\_DE\_PEAK}$ for G-2FP fades away, and that for G-3FP disappears. These peak electric field profiles of the devices support the above explanation for CE generation.

4.3 Specific On-Resistance and Drain-to-Source Breakdown Voltage

Table 2 shows R_{ON_SP}, BV_{DS_OFF}, and power FOM for GC-FFP, G-FFP, G-2FP, and G-3FP. R_{ON_SP} is calculated using I_{DS}, V_{DS} = 0.5 V, and the cell layout area at V_{GS} = 3.3 V (on-state operation voltage), and BV_{DS_OFF} is V_{DS} at J_D = 1 μA/mm^2 and V_{GS} = 0 V. The FOM is lower in the order of G-FFP, GC-FFP, G-2FP, and G-3FP. The highest FOM of G-FFP comes from the optimized characteristics of R_{ON_SP} vs. BV_{DS_OFF}. The FOM of G-2FP is just a little lower than that of GC-FFP due to a larger capacitance between the field plate and the drift region, C_{FD}, under the GFP2 of G-2FP especially, which increases the resistance in the drift region, namely raises R_{ON_SP}. The increase in C_{FD} also slightly increases the BV_{DS_OFF} of G-2FP because it enhances the RESURF in the drift region. (See Fig. 12.) The FOM of G-3FP is lower than that of G-2FP due to an even larger C_{FD} under the GFP3 of G-3FP. This larger C_{FD} further increases R_{ON_SP} and enhances the RESURF near the gate-side drift region edge, where the peak electric field in the minus x-direction, $E_{XX\_GE\_PEAK}$, decreases, leading to a little increase in the electric field in the x-direction near the GFP1 edge of G-3FP. (See Fig. 12.) This increase in the electric field reduces the BV_{DS_OFF} of G-3FP. The multi-step field plate of the proposed device reduces the FOM compared to the conventional device due to the larger C_{FD}, after all.

Table 2 R_{ON_SP}, BV_{DS_OFF}, and FOM depending on device structures.

LDMOS	R_{ON_SP} [mΩmm^2]	BV_{DS_OFF} [V]	FOM ($BV_{DS\_OFF}^2/R_{ON\_SP}$) [kW/mm^2]
GC-FFP	39.8	60.6	**92.3**
G-FFP	40.8	62.2	**94.8**
G-2FP	41.8	61.9	**91.7**
G-3FP	42.4	61.1	**88.1**

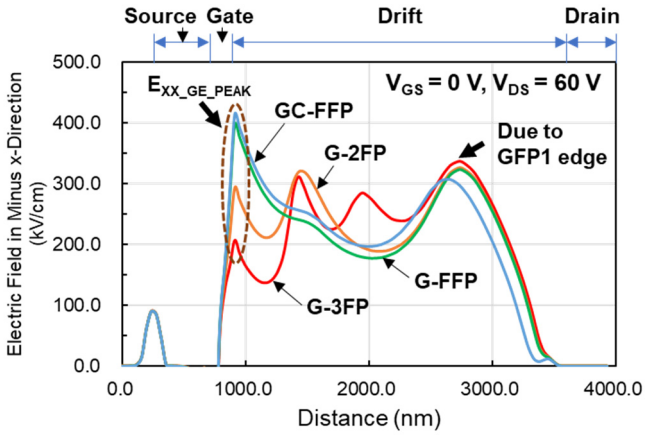


Fig. 12. Electric field profiles in the minus x-direction along the interface depending on device structures under V_{GS} = 0 V and V_{DS} = 60 V.

Fig. 13 shows hole current density distributions upon drain-to-source breakdown for GC-FFP, G-FFP, G-2FP, and G-3FP. The proposed device has a high hole current density region near the PBL2 edge, the breakdown location, the same as the conventional device upon the breakdown. Therefore, since both devices do not cause filamentation [12] due to a high current flowing in the drift region in

ESD (Electro Static Discharge) events, the ESD endurance level of the proposed device would be almost the same as that of the conventional device. However, in the case of repetitive ESD events, Fig. 12 indicates that the conventional one may damage the interface near the gate-side drift region owing to a high electric field (more than 400 kV/cm), but the proposed one does not. (The electric field of more than about 300 kV/cm in Silicon generates significant impact ionization.)

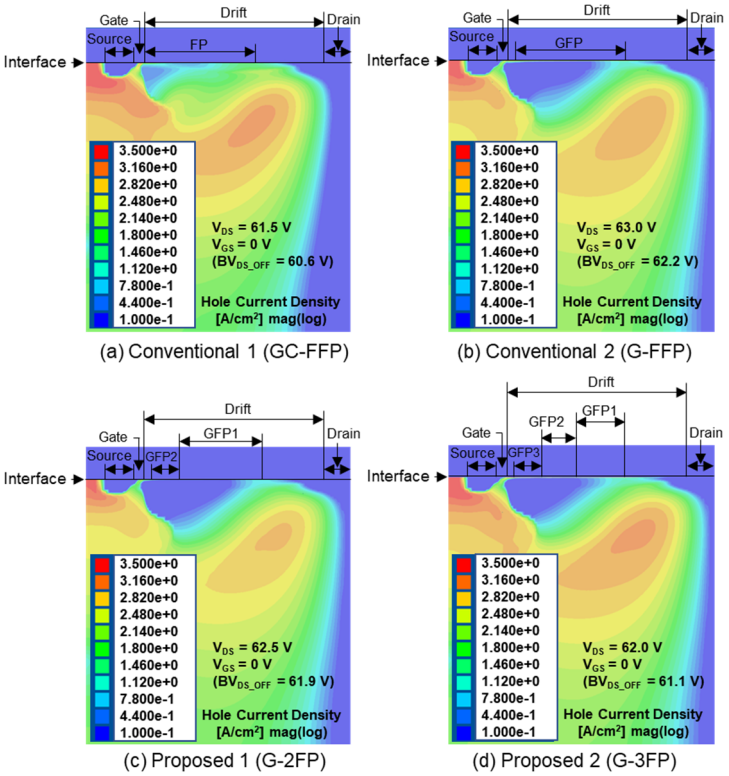


Fig. 13. Hole current density distributions upon drain-to-source breakdown depending on device structures.

4.4 Switching Loss

Table 3 shows the switching energy loss, E_{SW_LOSS}, for GC-FFP, G-FFP, G-2FP, and G-3FP. E_{SW_LOSS} includes the drain and the gate driving losses during turn-on and turn-off. E_{SW_LOSS} of G-FFP, G-2FP, and G-3FP is 53 %, 52 %, and 50 % of GC-FFP, respectively. The low Miller effect of G-FFP, G-2FP, and G-3FP with the grounded field plate reduces the switching loss significantly. The multi-step field plate increasing C_{FD} further reduces the switching loss [6].

Table 3 Switching loss depending on device structures.

LDMOS	GC-FFP	G-FFP	G-2FP	G-3FP
E_{SW_LOSS} (nJ/mm^2)	143.0	75.5	73.9	71.8

Fig. 14 shows the characteristics of the total power loss, P_{T_LOSS}, vs. switching frequency, f_{SW}, depending on duty ratio, D, for GC-FFP, G-FFP, G-2FP, and G-3FP. At D = 0.1, the P_{T_LOSS} of GC-FFP is higher than those of G-FFP, G-2FP, and G-3FP for $f_{SW} \gtrsim$ 200 kHz. Here the characteristics of G-FFP, G-2FP, and G-3FP are almost the same because the difference in the switching loss between them is slight. At D = 0.5, the P_{T_LOSS} of GC-FFP is higher than that of G-3FP for $f_{SW} \gtrsim$ 1MHz, and at D = 0.9, it is higher than that of G-3FP for $f_{SW} \gtrsim$ 1.8 MHz. The higher R_{ON_SP} of G-3FP than GC-FFP increases the conduction loss at a high D, increasing the crossover switching frequency between

GC-FFP and G-3FP characteristics for P_{T_LOSS} vs. f_{SW}. At D = 0.5 and 0.9, the characteristic for G-2FP is lower than that for G-3FP for 100 kHz ≤ f_{SW} ≤ 3 MHz due to lower conduction loss. The characteristic for G-FFP is further lower than that for G-2FP for the same reason. In short, as for the characteristics of P_{T_LOSS} vs. f_{SW}, G-3FP is superior to GC-FFP for f_{SW} ≳ 200 kHz at D = 0.1, f_{SW} ≳ 1 MHz at D = 0.5, and f_{SW} ≳ 1.8 MHz at D = 0.9. G-2FP has almost the same characteristics as G-3FP. However, the proposed device is slightly inferior to G-FFP for 100 kHz ≤ f_{SW} ≤ 3 MHz for D ≥ 0.5.

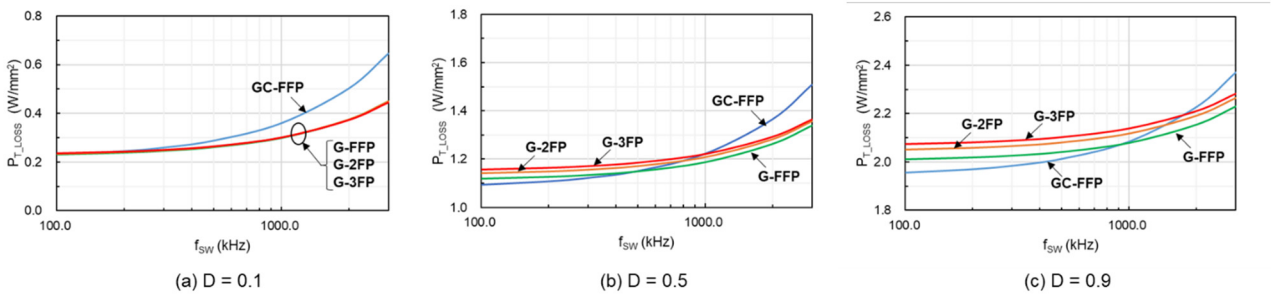


Fig. 14. P_{T_LOSS} vs. f_{SW} depending on device structures.

5. Conclusion

The proposed device (G-2FP and G-3FP) has higher hot carrier endurance than the conventional device (GC-FFP and G-FFP) due to enhanced RESURF near the gate-side drift region edge, in which G-3FP has much higher hot carrier endurance than G-2FP because GFP3 in G-3FP much enhances the RESURF. The enhanced RESURF also raises the BV_{DS_ON} (CE generation voltage) for the proposed device more than the conventional device. However, the power FOM of the proposed device is a little lower than that of G-FFP with optimized R_{ON_SP} vs. BV_{DS_OFF} characteristics. The proposed device may have higher ESD endurance than the conventional one because of the more enhanced RESURF and the breakdown location near the PBL2 edge upon the drain-to-source breakdown same as the conventional one. The switching loss of the proposed device is about 50 % of that of GC-FFP due to a much lower Miller effect, and it is lower than G-FFP due to a higher C_{FD} caused by the multi-step field plate. As for the P_{T_LOSS}, G-3FP is superior to GC-FFP for a high f_{SW} region: f_{SW} ≳ 1 MHz at D = 0.5, for example. G-2FP has almost the same characteristics as G-3FP. However, the proposed device is slightly inferior to G-FFP for a high D region: D ≥ 0.5 for 100 kHz ≤ f_{SW} ≤ 3 MHz, for example. The above indicates that the proposed device has high reliability to meet automotive applications used in harsh environments with a much lower switching loss. We can choose G-2FP or G-3FP by considering the specification that automotive applications require and the process cost.

Acknowledgements

We greatly appreciate AdvanceSoft Corporation for providing us with some licenses for using the 3D TCAD simulator. Japan Science and Technology Agency (National Research and Development Agency) assisted in developing this simulator using the A-STEP program.

Appendix

We derive α using the following equation expressing drain-to-source current, I_{DS}, vs. drain-source voltage, V_{DS}, characteristics in the linear region of a MOSFET [10].

$$I_{DS} = K'\left[(V_{GS} - V_T)V_{DS} - \frac{\alpha}{2}V_{DS}^2\right] \quad (2)$$

$$K' = \frac{\mu C_{OX} W}{L} \quad (3)$$

Here, μ is electron mobility in the n-channel inversion layer, C_{OX} gate oxide capacitance per unit area, W channel width, and L channel length. When applying Eq. (2) to the intrinsic MOSFET, Eq. (2) is as follows.

$$-J_S = K'/A_{CELL}\left[(V_{GS}-V_T)V_{DS\_INT}-\frac{\alpha}{2}V_{DS\_INT}^2\right] \tag{4}$$

Here, A_{CELL} is the cell area of the LDMOS transistor. First, we obtain two sets of $-J_S$ and V_{DS_INT} in the linear region from the simulation: ($-J_{S1}$, V_{DS_INT1}) and ($-J_{S2}$, V_{DS_INT2}) at V_{GS} = 4 V, for example. (See Fig. 5.) After applying the two sets to Eq. (4), eliminating K'/A_{CELL} from the two equations derives α as follows.

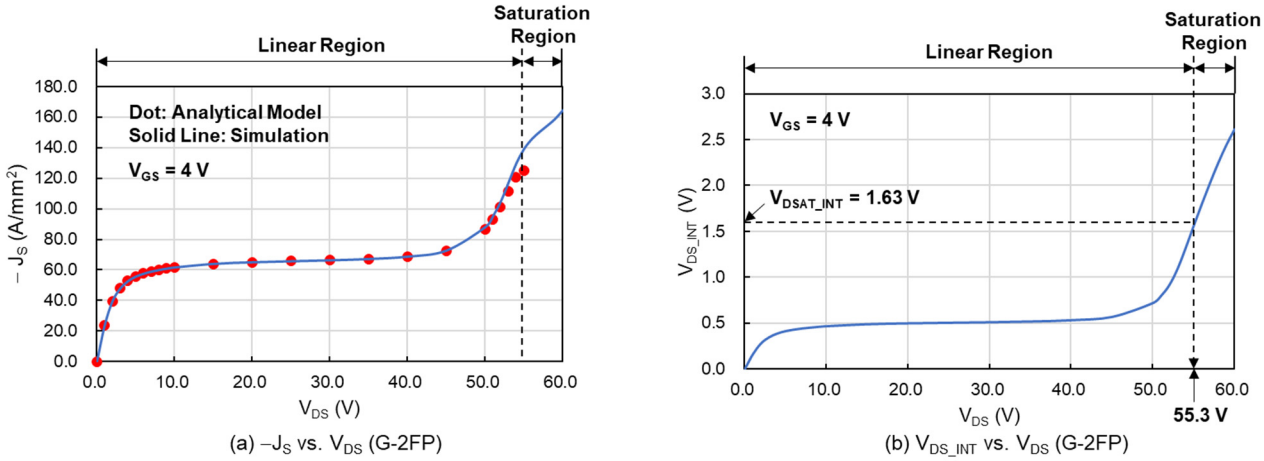
$$\alpha = \frac{2(V_{GS}-V_T)\left[V_{DS\_INT2}\left(\frac{J_{S1}}{J_{S2}}\right)-V_{DS\_INT1}\right]}{\left(\frac{J_{S1}}{J_{S2}}\right)V_{DS\_INT2}^2-V_{DS\_INT1}^2} \tag{5}$$

K'/A_{CELL} can be obtained using α and one set ($-J_{S1}$, V_{DS_INT1}) at V_{GS} = 4 V.

$$K'/A_{CELL} = \frac{-J_{S1}}{(V_{GS}-V_T)V_{DS\_INT1}-\frac{\alpha}{2}V_{DS\_INT1}^2} \tag{6}$$

Second, we obtain the relationship between V_{DS_INT} and V_{DS} from the characteristic of I_{DS} vs. V_{DS} at V_{GS} = 4 V of the LDMOS transistor by the simulation.

Using α and K'/A_{CELL} in Eq. (4), we can obtain the characteristic of $-J_S$ vs. V_{DS_INT} at a V_{GS} in the linear region. Further, using the relationship between V_{DS_INT} and V_{DS}, we can transform $-J_S$ vs. V_{DS_INT} to $-J_S$ vs. V_{DS} characteristics. Fig. 15 shows the characteristics of $-J_S$ vs. V_{DS} and V_{DS_INT} vs. V_{DS} at V_{GS} = 4 V for G-2FP. As for the $-J_S$ vs. V_{DS} characteristic, the analytical model explained here fits the simulation result well. Applying V_{DSAT_INT} obtained by Eq. (1) to the V_{DS_INT} vs. V_{DS} characteristic, we can find the saturation voltage of V_{DS} (55.3 V in this case). Table 4 shows α, K'/A_{CELL}, V_{DSAT_INT} at V_{GS} = 4 V, and V_{DS} at V_{DS_INT} = V_{DSAT_INT} under V_{GS} = 4 V for GC-FFP, G-FFP, G-2FP, and G-3FP. Each of α, K'/A_{CELL}, and V_{DSAT_INT} at V_{GS} = 4 V is almost the same between GC-FFP, G-FFP, G-2FP, and G-3FP, because all the devices have the same impurity profiles. V_{DS} at V_{DS_INT} = V_{DSAT_INT} under V_{GS} = 4 V of G-3FP is higher than any other devices due to its lowest V_{DS_INT} in all the devices. (See Fig. 5.) V_{DS} at V_{DS_INT} = V_{DSAT_INT} under V_{GS} = 4 V of G-2FP is lower than G-3FP but higher than GC-FFP and G-FFP depending on V_{DS_INT}.



(a) $-J_S$ vs. V_{DS} (G-2FP) (b) V_{DS_INT} vs. V_{DS} (G-2FP)

Fig. 15. $-J_S$ vs. V_{DS} and V_{DS_INT} vs. V_{DS} characteristics.

Table 4 α, K'/A_{CELL}, V_{DSAT_INT} at V_{GS} = 4 V, and V_{DS} at V_{DS_INT} = V_{DSAT_INT} under V_{GS} = 4 V depending on device structures.

LDMOS	α	K'/A_{CELL} [A/V^2/mm^2]	V_{DSAT_INT} [V] at V_{GS} = 4 V	V_{DS} [V] at V_{DS_INT} = V_{DSAT_INT} under V_{GS} = 4 V
GC-FFP	1.83	52.19	1.62	54.2
G-FFP	1.83	52.13	1.61	53.8
G-2FP	1.81	52.06	1.63	55.3
G-3FP	1.80	51.68	1.64	56.3

References

[1] J. Matsuda, M. Kamiyama, N. Tsukiji, J. Kojima and H. Kobayashi, "Proposal of High Reliability LDMOS Structure", ***Proceedings of 7th AMDE*** (Kiryu, Japan) Nov. P8-22, 2015.

[2] J. Kojima, J. Matsuda, M. Kamiyama, Nobukazu Tsukiji and H. Kobayashi, "Optimization and analysis of high reliability 30‐50V dual RESURF LDMOS", ***Proceedings of 13th ICSICT*** (Hangzhou, China) Oct. 2016.

[3] J. Matsuda, J. Kojima, M. Kamiyama, N. Tsukiji and H. Kobayashi, "A Low Switching Loss 40 V Dual RESURF LDMOS Transistor with Low Specific On-Resistance", ***Proceedings of ICMEMIS2017*** (Kiryu, Japan) Nov. I01-05, 2017.

[4] J. Matsuda, J. Kojima, N. Tsukiji, M. Kamiyama and H. Kobayashi, "Low Switching Loss and Scalable 20-40 V LDMOS Transistors with Low Specific On-Resistance", ***Proceedings of ICTSS2018*** (Kiryu, Japan) Apr. I03-02, 2018.

[5] H. Y. Du, J. Matsuda, A. Kuwana and H. Kobayashi, "Analysis of Switching Characteristics of Dual RESURF 40 V N-LDMOS Transistor with Grounded Field Plate", ***Proceedings of ICTSS*** (Kiryu, Japan) Dec. IPS-02-a, 2021.

[6] H. Y. Du, J. Matsuda, A. Kuwana, and H. Kobayashi, "Low Switching Loss Dual RESURF 40 V N-LDMOS with Grounded Field Plate for DC-DC Converters", ***Proceedings of MWSCAS2022*** (Fully Virtual and On-line) Aug. 2022.

[7] S. Reggiani, G. Baccarani, E. Gnani, A. Gnudi, M. Denison, S. Pendharkar, R. Wise, and S. Seetharaman : "Explanation of the Rugged LDMOS Behavior by Means of Numerical Analysis", ***IEEE Transactions on Electron Devices***, Vol. 56, No. 11 pp.2811-2818, 2009.

[8] K. Yamaguchi, M. Harada, T. Kuwabara and Y. Ohkura, "Device Simulation", ***Advance Simulation*** (AdvanceSoft Corporation), Vol. 21, pp. 39-69, 2015.

[9] K. Yamaguchi, "A Mobility Model for Carriers in the MOS Inversion Layer", ***IEEE Transactions on Electron Devices***, Vol. 30, No. 6, pp. 658-663, 1983.

[10] Y. Tsividis and C. McAndrew, "The four-Terminal MOS Transistor in ***Operation and Modeling of the MOS Transistor Third Edition***, Oxford University Press, (New York, USA), pp. 151-242, 2011.

[11] C. T. Kirk, "A Theory of Transistor Cutoff Frequency (ft) Falloff and High Current Densities", ***IRE Transactions on Electron Devices***, Vol. 9, No. 2, pp.164–174, 1962.

[12] S. Pendharkar, P. Hower, R. Steinhoff, J. Brodsky, J. Devore and B. Grose, "Using Two-Dimensional Filament Modeling to Predict Ldmos and Scrldmos Behavior under High Current ESD Conditions", ***Proceedings of ISPSD 2001***, (Osaka, Japan) Jun. pp. 161 -164, 2001.