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Single-Inductor Dual-Output Converters With PWM, Hysteretic, Soft Switching and Current Controls

Yifei Sun[a], Yasunori Kobori[b], Minh Tri Tran[c]
Anna Kuwana[d] and Haruo Kobayashi[e]

Division of Electronics and Informatics, Faculty of Science and Engineering, Gunma University
1-5-1 Tenjincho, Kiryu-shi, Gunma, 376-8515, Japan

[a]< t172d004@gunma-u.ac.jp >, [b]<kobori@gunma-u.ac.jp>, [c]< t182d002@gunma-u.ac.jp >,
[d]<kuwana.anna@gunma-u.ac.jp>, [e]<koba@gunma-u.ac.jp>

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Abstract. This paper reviews some kinds of our investigated single-inductor dual-output (SIDO) DC-DC switching converters with PWM control, ripple-based hysteretic control and soft switching control. First, buck type SIDO converters with PWM control are explained with the exclusive control method. Second, hysteretic controlled SIDO converters with the triangular signal generated by the CR-circuit connected across the inductor, and third, soft-switching SIDO converters with the half/full wave type resonance and with ZVS-PWM resonant control, while last the current controlled converters are presented. The novel technologies of these SIDO converters are described with circuit topologies, operation principles, simulation results and experimental results. Also their comparison is discussed.

1. Introduction

Many DC-DC converters are widely used in electronic devices, from cell phones to large manufacturing machinery, and there the weight and volume of the circuits are very important items as well as the efficiency. In many applications, several kinds of supply voltages are required for analog circuits and digital circuits in order to improve the efficiency of the circuits. For analog circuits, in order to prevent cross-talk, it is necessary to separate power supplies for an oscillator circuit and a weak radio wave receiver circuit even with the same voltage.

Therefore, we propose the single-inductor dual-output (SIDO) converter to reduce the number of inductors that are difficult for on-chip integration and have large volume and weight. In this paper, several kinds of novel SIDO switching converters are described with their operating principles and simulation results. Their experimental results are also shown to verify their basic operation and performance.

2. SIDO DC-DC Converters with Exclusive Control Method

2.1 Basic DC-DC Buck Type Switching Converter

Fig. 1 shows the basic block diagram of the buck type DC-DC converter [1-3] with the Pulse Width Modulation (PWM) signal control and Fig. 2 shows its main signals. This converter consists of the power and control stages. The power stage contains a main power switch, a freewheeling diode, an inductor and an output capacitor. The main switch is controlled by the PWM signal from the control stage, which is composed of an operational amplifier, a comparator and a reference voltage source. The comparator generates the PWM signal by comparing the saw-tooth signal and the amplified error voltage ΔV (Fig. 2). In the buck type DC-DC converter, the output voltage V_o can be expressed by the following equation using the input voltage V_i and the ON/OFF duty ratio D.

$$V_O = D \times Vi \tag{1-1}$$

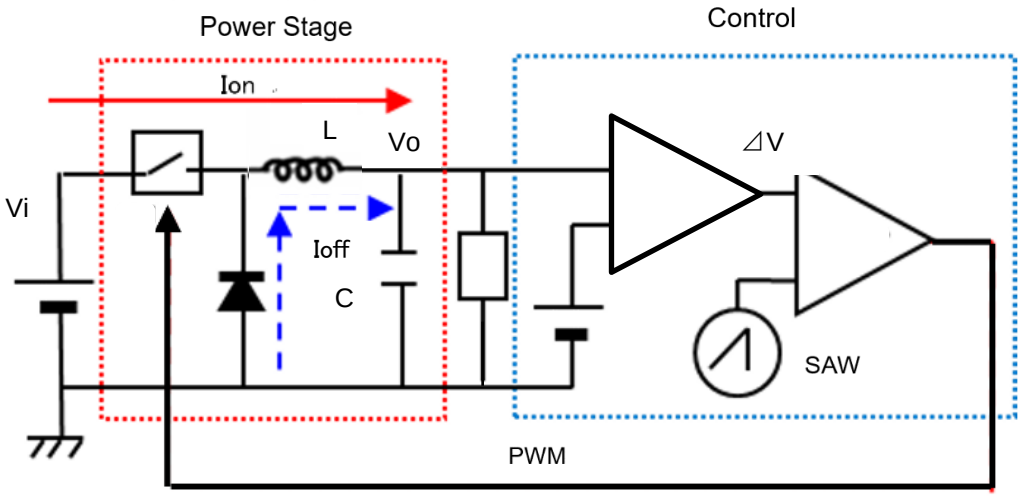


Fig. 1 Buck converter with the PWM signal. PWM=pulse Width Modulation, SAW=Sawtooth signal, ⊿V=Amplified error voltage

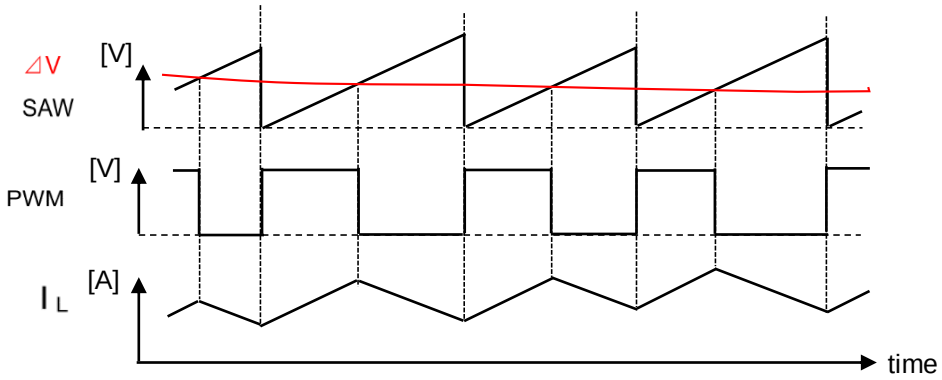


Fig. 2 Illustrated signals of the buck converter. I_L = Inductor current

2.2 SIDO Converters with Exclusive Control Method

Fig. 3 shows the SIDO buck type converter with PWM control [4,5]. The SIDO converter has the single power stage, two sub-converters, a comparator, a selector and a PWM generator. The sub-converter consists of an output capacitor, a select switch and an operational amplifier. Fig. 4 shows the waveforms of the SIDO converter. Two sub-converters are selected to be controlled by the SEL signal which is supplied from the comparator; it compares two amplified output error voltages$\Delta V1$ and$\Delta V2$. When the error voltage$\Delta V1$ is larger than$\Delta V2$, the SEL signal is high and the select switch S_1 is selected to be ON and the select switch S_2 is OFF. The power from the power stage is supplied to the sub-converter 1 and the voltage V1 goes up. In this case, the main power switch S_0 in the power stage is controlled by the PWM signal, which is supplied from the comparator in the PWM generator.

In the SIDO converter, one of the two sub-converters is supplied with the power exclusively. We call this control method “Exclusive Control”. The exclusive control is independent of the difference of the output voltages or the output currents. The comparator 1 compares two error voltages.

2.3 Simulation Results of SIDO Converter

Simulation results of the SIDO buck converter are shown in from Fig. 5 to Fig. 7, and the parameters in this simulation are shown in Table 1. Here output voltages V1 and V2 are 6.0V/5.0V and output

currents are I1=I2=0.5A, typically. In Fig. 5, I1 increases to 1.0A from time 3ms to 4ms, while I2 increases to 1.0A from time 5ms to 6ms. Fig. 6 shows the output ripples of V1 and V2 which are about

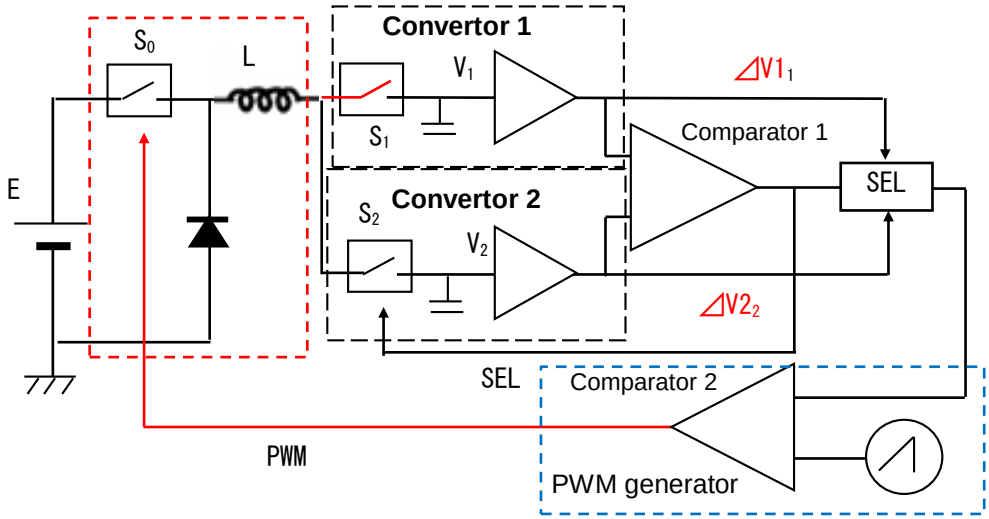


Fig. 3 Circuit of the SIDO converter. SIDO=Single-Inductor Dual-Output, SEL=Select signal

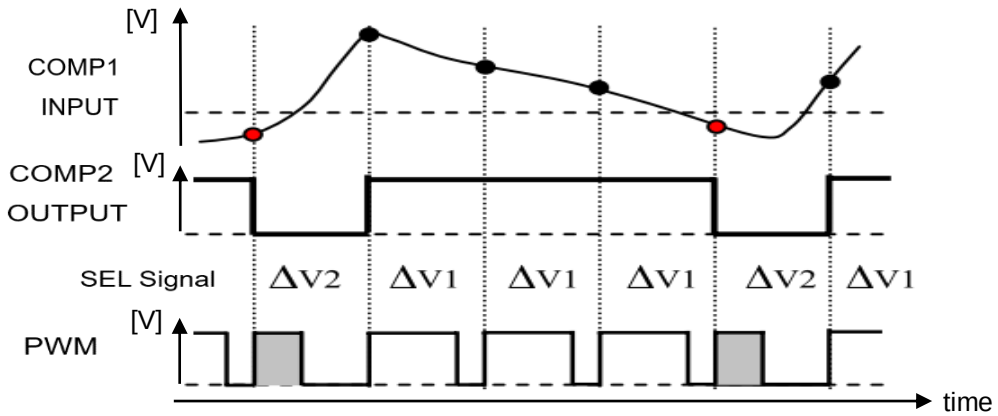


Fig. 4 Illustrated signals of COMP I/O, PWM and SEL. COMP=Comparator

10 mVpp when I1=1.0A and I2=0.5A. The duty ratio of the select signal SEL is about 25%. Usually, this SEL duty ratio is about 50% when I1=I2. Fig. 7 shows the transient responses when the current change is 1.0A/0.5A in each output current. Here the red solid arrow shows the self-regulation and the blue dashed one shows the cross-regulation. The under/over-shoot of the output voltage is less than 20 mV in each response.

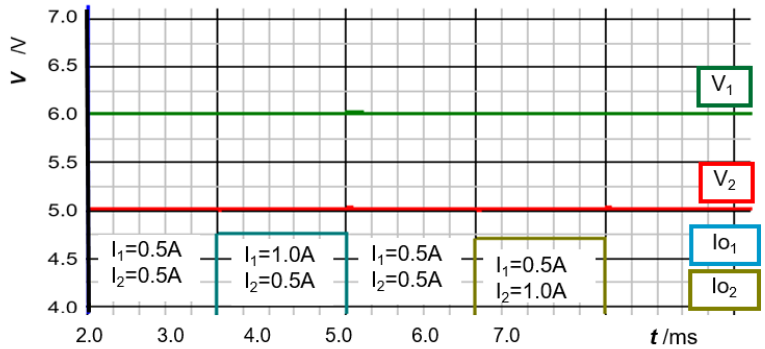


Fig. 5 Simulation result of SIDO converter.

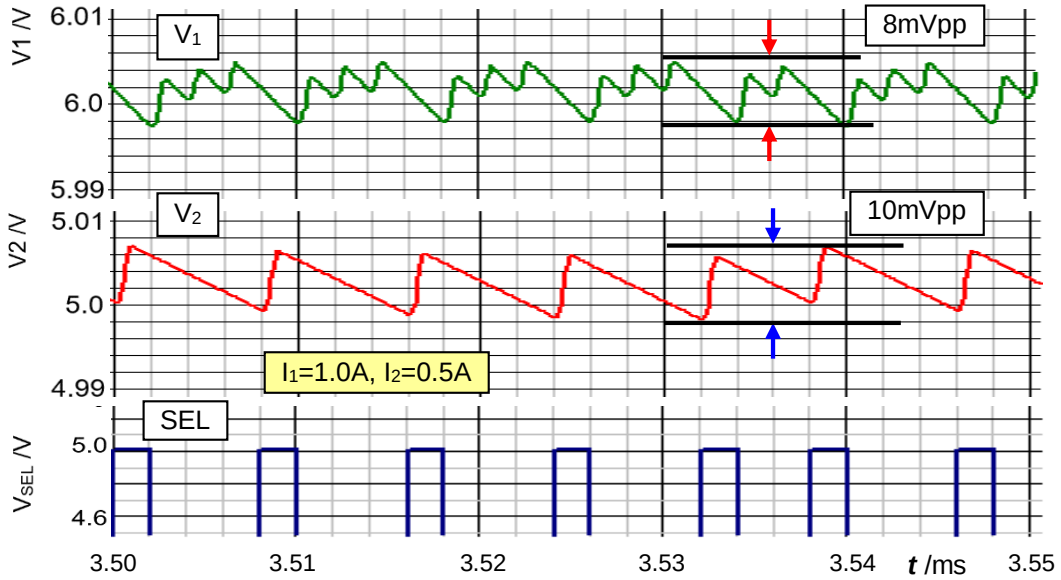


Fig. 6 Output ripple of SIDO converter.

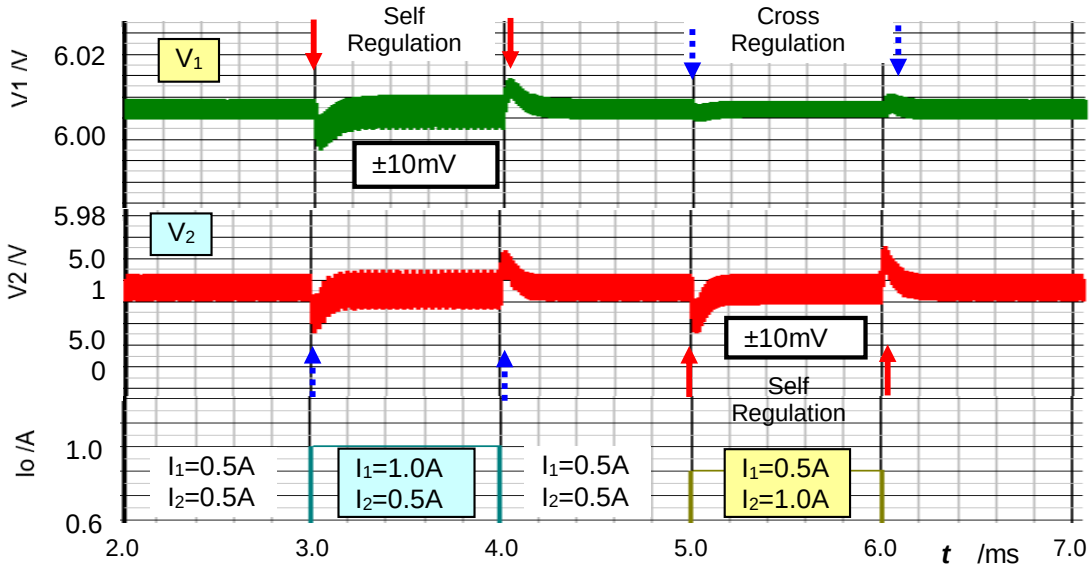


Fig. 7 Transient responses for current step.

Table 1 Parameters of SIDO converter

Parameter	***Value***
E	9.0 [V]
L	0.2 [μH]
C	470 [μF] each
V_1	6.0 [V]
V_2	5.0 [V]
I_1/I2	1.0 / 0.5 [A]
Fck	500 [kHz]

2.4 Experimental Results of SIDO Converter

Fig. 8 shows the experimental results of the SIDO converter. Here, the static output current is I1=I2=0.25A, and I2 changes to 0.50A periodically. The static voltage ripples of V1 and V2 are about 20 mVpp and the transient responses are less than 10 mV. The duty ratio of the SEL signal is almost 50%.

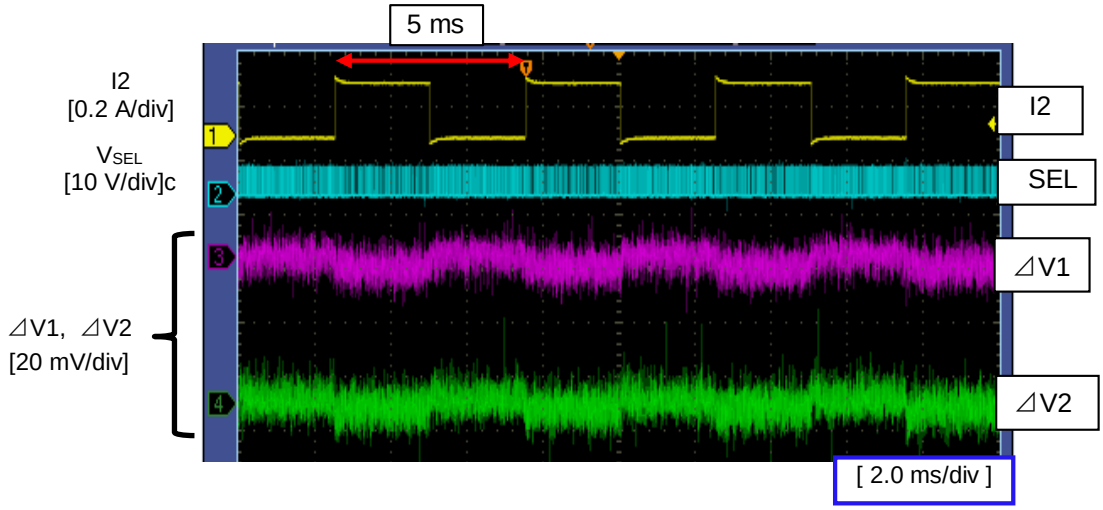


Fig. 8 Experiment results of output ripple of SIDO hysteretic converter

3. SIDO Hysteretic Converter with Ripple-based Control

3.1 Basic Buck Type Hysteretic Converter

Fig. 9 shows a basic buck type hysteretic converter with the ripple-based control, which consists of the power stage and the comparator. Notice that there is no amplifier, and the output voltage Vo is directly compared with the reference voltage Vref. Fig. 10 shows the timing chart. When Vo becomes lower than Vref, the output signal CONT of the comparator turns high with a slight delay. Then this CONT signal controls the main switch ON, and the source energy is supplied to the capacitor C and the load resistor R through the inductor L at time B with some delay Td_{on}. When Vo becomes higher than Vref at time C, the CONT signal turns low and the switch SW turns OFF with a slight delay, so that the output voltage Vo is a little bit overcharged. The inductor current starts to decrease at time D with some delay Td_{off} and the current is supplied from the diode.

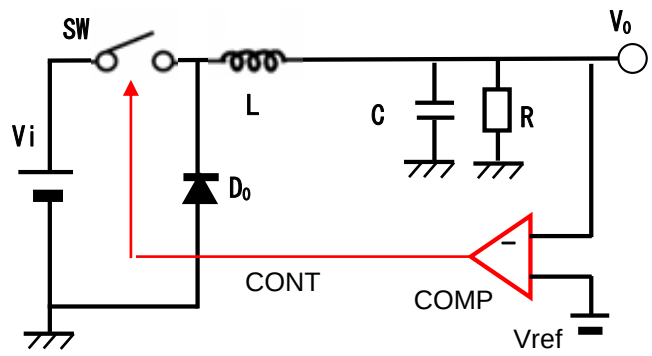


Fig. 9 Circuit of basic hysteretic converter. CONT=Control pulse, Vref=Reference voltage

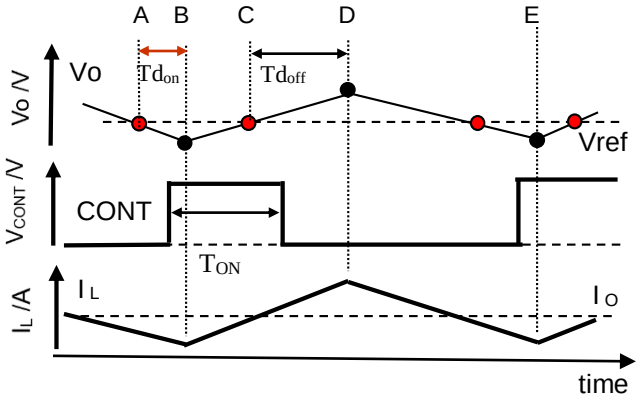


Fig. 10 Illustrated signals of hysteretic converter.

During the time B and D, the rising current of the inductor $I_{LR}(t)$ is expressed in (3-1).

$$I_{LR}(t) = (Vi - Vo)\cdot t / L \quad (3\text{-}1)$$

The peak value of the current I_D at time D is expressed in (3-2) using the period T_{ON}.

$$I_D = I_{LR}(T_{ON}) = (Vi - Vo)\ T_{ON} / L \quad (3\text{-}2)$$

The falling current $I_{LF}(t)$ is expressed in (3-3) and the period T_F from D to E is solved as (3-5). The value of L is usually about 1μH in order to make this overcharge small.

$$I_{LF}(t) = I_D - Vo\cdot t / L \quad (3\text{-}3)$$

$$I_{LF}(T_F) = (Vi - Vo)\ T_{ON} / L - Vo\cdot T_F / L = 0 \quad (3\text{-}4)$$

It follows from (3-3), (3-4) that we have :

$$T_F = \{(Vi - Vo)/Vo\}\cdot T_{ON} = (Vi / Vo - 1\ )\ T_{ON} \quad (3\text{-}5)$$

Fig. 11 shows the simulated output voltage rippleΔVo for the output current stepΔIo=0.5A and Table 2 shows the parameters of this hysteretic converter. The hysteretic converter usually responds quickly to load change and its voltage ripple is very small. In this simulation, the ripple is smaller than 3 mVpp at Io=0.5A and about 7mVpp at Io=1.0A as shown in Fig. 11. The overshoot is about 1mV when the output current step is 0.5A.

Basic hysteretic converters have some demerits. One is that the output ripple ΔVo increases as the output current increases as shown in Fig. 11. Second one is that the operating frequency is very high and it varies with the output current change, which causes the large Electro-Magnetic Interference (EMI) noise. In Fig. 11, the frequency is higher than 150kHz when Io=0.5A. Third one is that the loop gain is very low because of no amplifier as shown in Fig. 9. The low loop gain makes the offset of the output voltage Vo. Last one is that this type of the hysteretic converter needs some voltage ripple because it is difficult to detect the voltage ripple when the ripple is reduced by replacing aluminum electrolytic capacitors with ceramic capacitors.

Table 2 Parameters of hysteretic converter

Parameter	***Value***
Vi	9.0 [V]
L	1.0 [μH]
C	470 [μF]
V_o	5.0 [V]
I_o	1.0 / 0.5 [A]

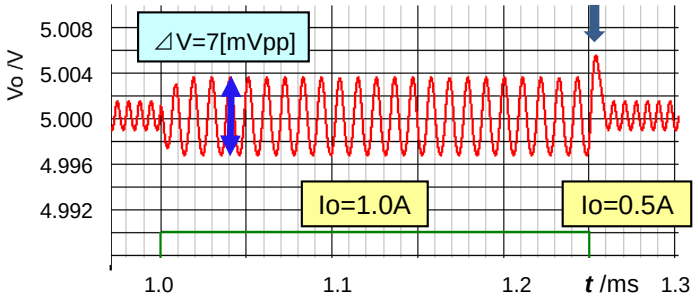


Fig. 11 Output ripple of hysteretic converter.

3.2 Hysteretic Converter with Triangular Signal

To amplify the ripple for its detection by the comparator, the triangular signal is generated at the CR circuit across the inductor (Fig. 12). A CR circuit and the amplifier to the basic hysteretic converter shown in Fig. 9. The error of the output voltage is amplified and compared with the triangular signal to generate the PWM signal, which controls the main switch SW to regulate the output voltage Vo.

The CR circuit integrates the inductor voltage in time, and generates the triangular signal which is larger than the output voltage ripple. In this control method, the control frequency depends on the time constant C_TR_T and the output current Io as well as the hysteresis voltage of the comparator. Here, R_T is 470 [kΩ] and C_T is 1.0 [nF]

Fig. 13 shows the simulation results of the output ripple and the transient response with the output current change. The voltage ripple at the steady state is about 5mVpp at Io=1.0A and the over/under-shoots are about +/- 4mV when Io changes from 0.5A to 1.0A and vice versa. The control frequency is about 360kHz.

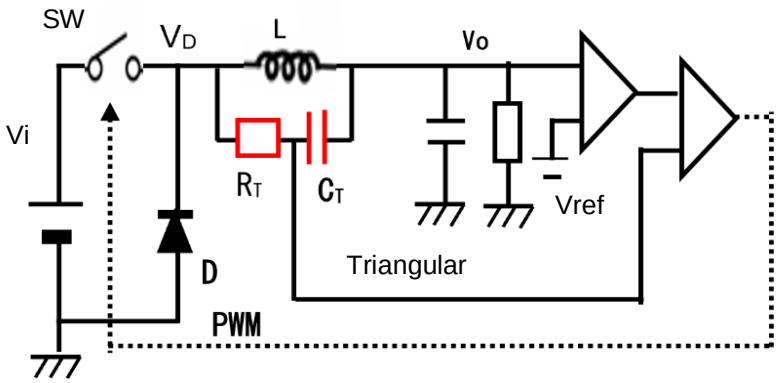


Fig. 12 Hysteretic converter with triangular.

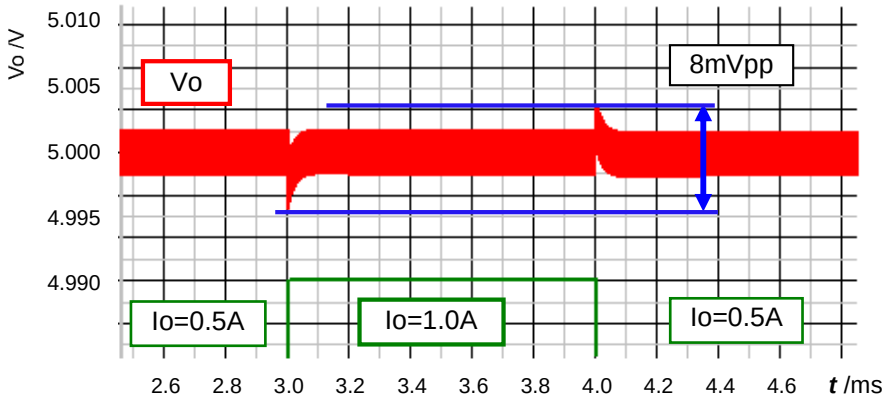


Fig. 13 Output ripple with current step.

3.3 SIDO Converter with Hysteretic Control

Fig. 14 shows the SIDO buck converter [6,7] with the triangular signal across the inductor. There are two sub-converters connected with the main power-stage, a comparator, a switch to select the PWM signal and the CR circuit for generating the triangular signal synchronized with the PWM signal. One of these sub-converters are selected to supply the power with the exclusive control method. In the next PWM cycle, one of two sub-converters is selected by SEL signal, whose error voltage ΔVo is larger than the other. The PWM signal is also selected by SEL signal.

In this SIDO converter, the CR circuit to generate the triangular signal is not connected across the inductor. One side of the CR circuit is connected to the output terminal of Vo1. The reason is because the voltage of the output terminal of the inductor changes according to the SEL signal which selects the differential output voltage Vo1 or Vo2. The capacitor C of the time constant CR must be connected to the stable voltage, for example Vo1, Vo2 or other stable terminals. This triangular signal is supplied to two comparators in both sub-converters to generate PWM signals. Here, Vi=10V, V_1=5.0V, V_2=4.5V, L=1.0uH, C=470uF and the operating frequency is about 500kHz.

In Fig. 14, the switch in the sub-converter 1 is replaced with the diode. When the SEL signal is high, the switch SW2 is ON and the sub-converter 2 is selected to be served because the diode in the sub-converter 1 is OFF. In this converter, Vo1 is set to be higher than Vo2. When the SEL signal is low, the switch SW2 is OFF and the sub-converter 1 is served through the diode.

Fig. 15 shows the simulation results of the output voltage ripples. The steady-state ripples are about 2mVpp when the output currents I1=I2=0.5 A. The over/under-shoots are less than 10 mV with output current steps ±0.5 A. In this circuit, the time constant CR of the triangular signal is about 4ms.

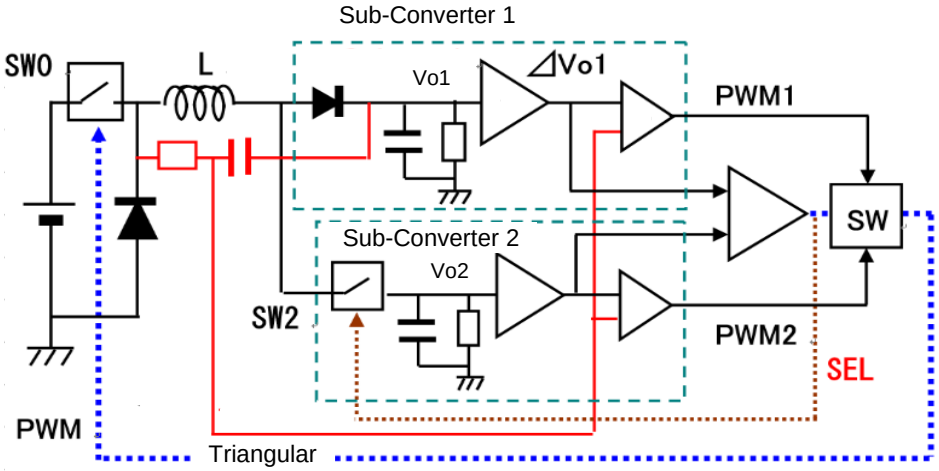


Fig. 14 SIDO Converter with hysteretic control.

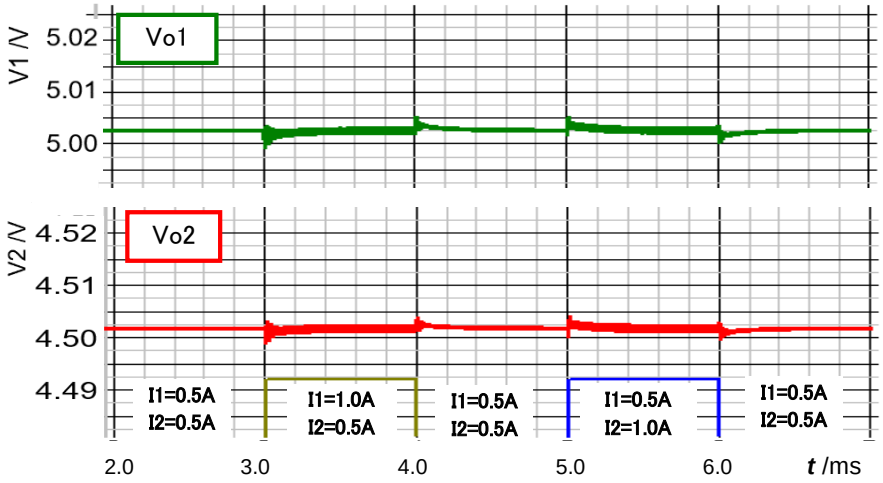


Fig. 15 Output ripples of SIDO converter.

3.4 Experimental Results of SIDO Hysteretic Converter

Fig. 16, 17 and 18 show the experimental results of the SIDO hysteretic converter with the parameters in Table 3. Fig. 16 shows two output voltages, which have large spike noises of about 200~350mVpp. Since the circuit is implemented on a universal board with discrete components and the impedance of the ground lines is estimated to be very large. Noises from the switching signals can appear in the ground lines or the signal wires. The measured voltage ripples without these spike noises are about 50mVpp, which is much larger than the simulation results.

In this circuit, the operational frequency (Fop) is set to low about 60 kHz because of the spike noises, and the amplitude of the ripples in the buck converter is inversely proportional to square of the operating frequency (Fop). The Fop of the simulation circuit is 500 kHz and the frequency ratio is about 8. So the amplitude of the measured ripple in the experiment is reasonable. In Fig. 16, the current I1 is changed with 0.2A step, and the cross-regulation or the self-regulation is very small.

Fig. 17 shows the experimental signals of the SIDO converter; the voltage (V_L) across the inductor, the SEL signal, the PWM signal and the triangular signal. The OFF timing of the PMOSFET switch is

much delayed and the amplitude of the triangular signal is about 4 Vpp which is synchronized with the PWM signal. The duty of SEL signal is about 50% because of the good balance of two output currents. The currents to sub-converters are clearly separated by the SEL signal in Fig.18. The current I1 flows when the SEL signal is low and the switch SW2 is OFF.

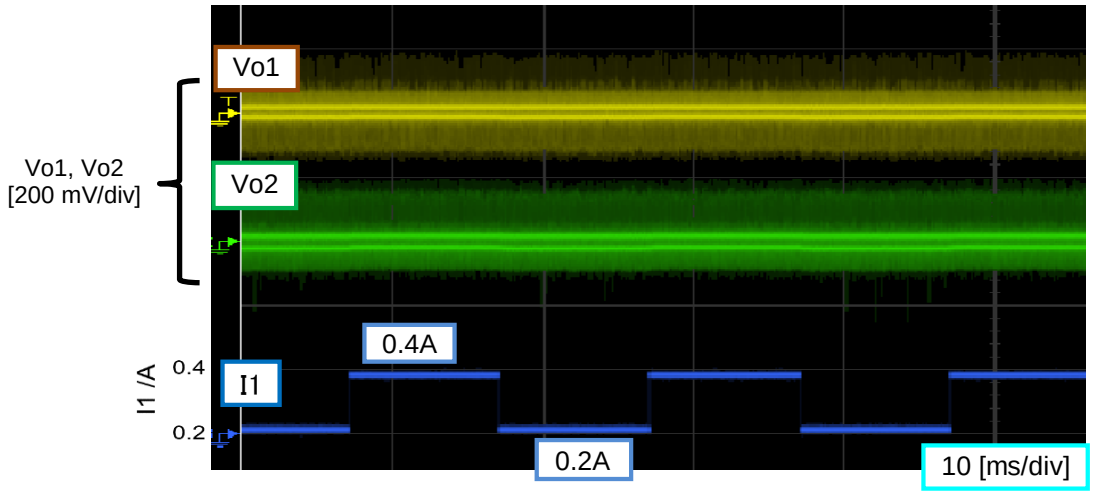


Fig. 16 Experimental output voltages of SIDO hysteretic converter.

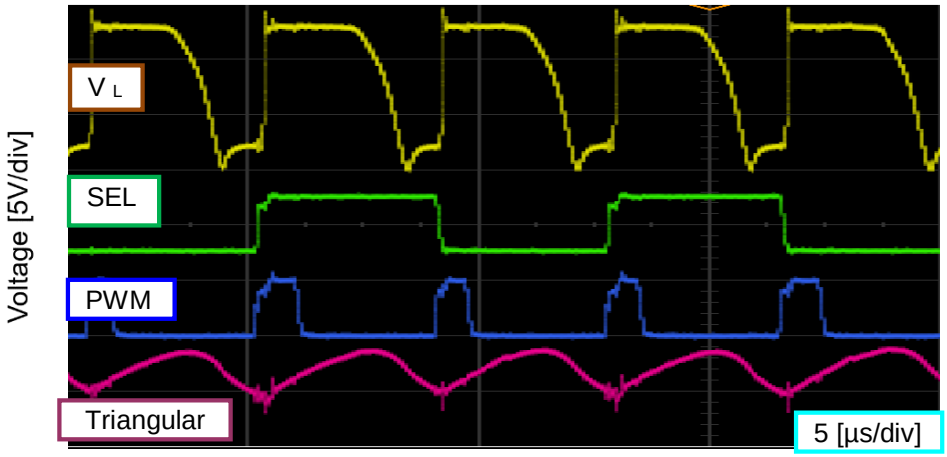


Fig. 17 Experimental waveforms of SIDO hysteretic converter.

Table 3 Parameters of SIDO converter

Parameter	***Value***
E	10 [V]
V_1	5.0 [V]
V_2	4.5 [V]
I_1, I_2	0.2 [A]
L	10 [µH]
Co	1,000 [µF]
R	4.0 [kΩ]
C	1.0 [nF]
Fck	60 [kHz]

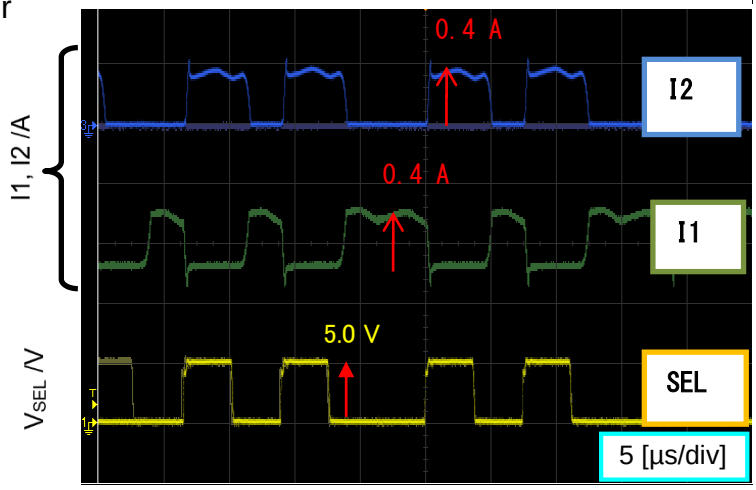


Fig. 18 Experimental output current of SIDO hysteretic converter

Fig. 17 shows the experimental signals of the SIDO converter; the voltage (V_L) across the inductor, the SEL signal, the PWM signal and the triangular signal. The OFF timing of the PMOSFET switch is much delayed and the amplitude of the triangular signal is about 4 Vpp which is synchronized with the PWM signal. The duty of SEL signal is about 50% because of the good balance of two output currents. The currents to sub-converters are clearly separated by the SEL signal in Fig.18. The current I1 flows when the SEL signal is low and the switch SW2 is OFF.

4. Resonant SIDO Converter with ZVS-PWM Control

4.1 Basic ZVS-PWM Controlled Resonant Converter

Fig. 19 shows the basic Zero Voltage Switching (ZVS)-PWM converter with the half-resonant control. This converter adds a resonant capacitor Cr and a ZVS detection comparator to the typical buck converter. The capacitor Cr is connected to the diode in parallel. The ZVS detection comparator is used to compare the voltages of Vsw and Vin.

Fig. 20 shows simulation results of the steady-state waveforms of the basic buck converter with ZVS-PWM control. When Vsw becomes higher than Vin at the start timing in state 1, the output of the ZVS detection comparator turns high, and a Flip-Flop (FF) becomes a SET state by receiving the high signal from this comparator. Then the main switch M1 turns ON. In this way, the switch MOSFET M1 keeps ON state and the current of the inductor increases as shown in Fig. 20. Thereafter the output voltage Vo becomes higher than the reference voltage Vref and the amplified error voltage is compared with the saw-tooth SAW signal. As Vo increases, the output of the amplifier decreases. Then the output of the PWM comparator turns high and the FF is reset to make its output turn low at state 2.

Detailed description of the operation is as follows: (See Fig. 20)

(1)During State 1, the PWM signal is high and M1 turns ON. In this period, the terminal voltage Vsw is equal to Vin. In addition, the current IL increases at the rate of (Vin-Vo) / L. Cr is charged to Vin during this period.

(2)During State 2, the PWM signal is low, and M1 turns OFF. In this period, D1 turns OFF, and the current IL is supplied to the output by Cr which is charged during State 1. The voltage Vsw gradually decreases due to the current supply from Cr. Finally, the voltage Vsw decreases to negative voltage until D1 turns ON.

(3)During State 3, the voltage Vsw is negative and D turns ON. The inductor current IL flows through the diode from GND. The current IL decreases at the rate of Vo/L. Cr is charged to a negative voltage equal to the forward bias voltage of D1.

(4)During State 4, the current IL is negative and D1 turns OFF. The current IL flows from Co to Cr to make the voltage Vsw increase from negative (about -0.7V) to positive voltages gradually with supply current to Cr. Then, the voltage Vsw reaches Vin and the ZVS detection comparator outputs a high signal. Then M1 turns ON and the state returns to State 1.

A resonant switching converter is well known as a very small switching loss configuration. In this operation, the main switch M1 turns ON at the timing that Vin=Vsw as shown in Fig. 20, which means that the voltage across the switch M1 is zero and there is no switching loss. Of course, when M1 turns OFF, the capacitance Cr keeps the voltage Vsw=Vin. As a result, the switching losses are greatly reduced with the ZVS operation. Table 4 shows the parameters of this ZVS-PWM converter.

Fig. 22 shows the measured waveforms of the voltage across the switch Vsw and the current through the switch Isw in our experiment. Fig. 22 (a) shows ones in the normal buck converter, and Fig.22 (b) shows in this ZVS-PWM buck converter, when the switch turns OFF. In the normal converter, there is much overlapped between Vsw and Isw, which causes switching loss. However, in ZVS-PWM converter, there is no overlapping.

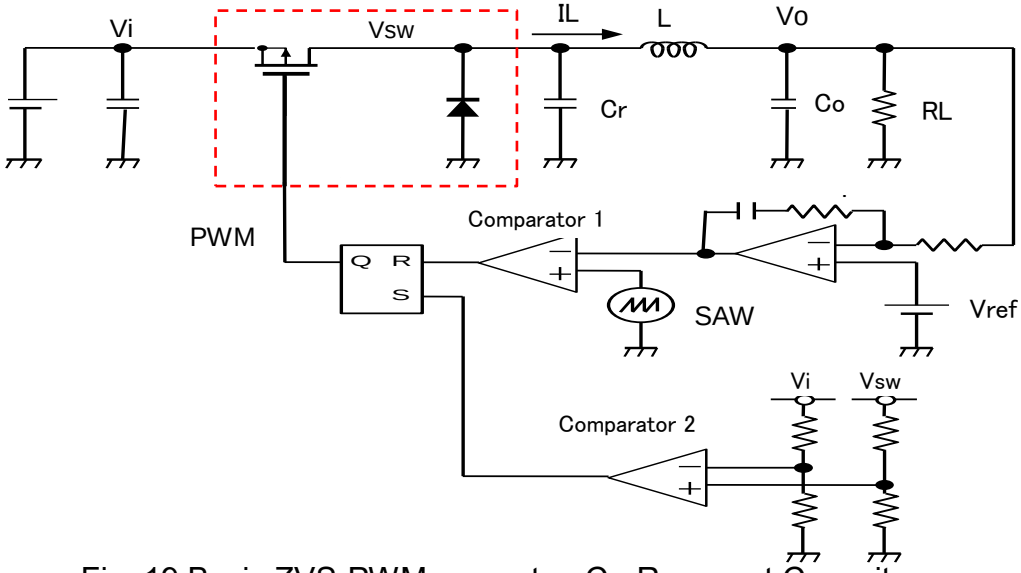


Fig. 19 Basic ZVS-PWM converter. Cr=Resonant Capacitor

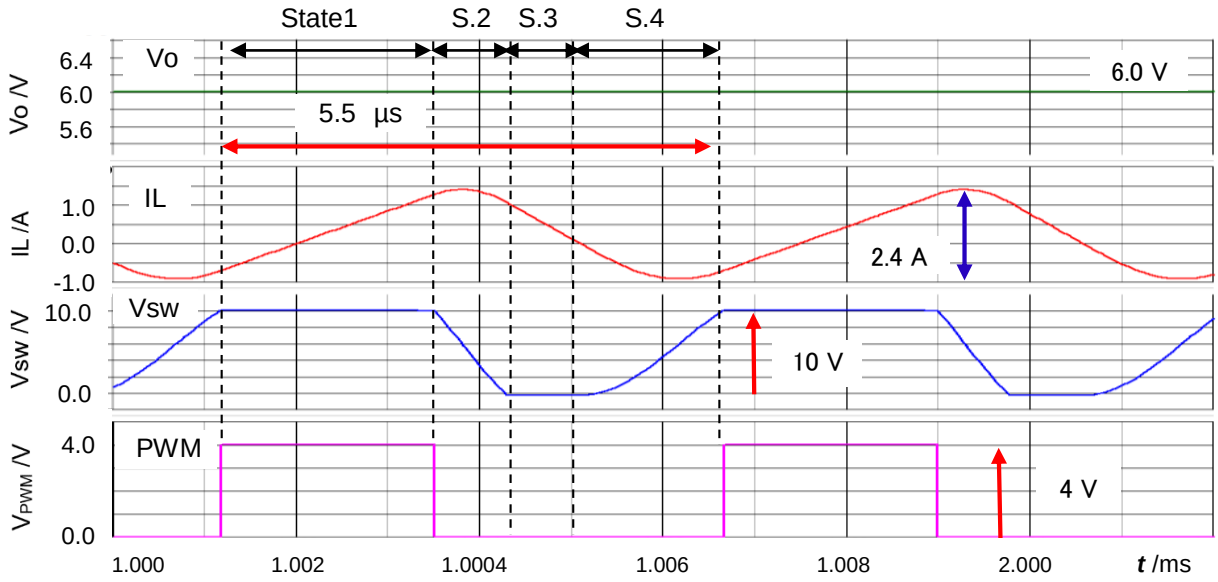


Fig. 20 Waveform of ZVS-PWM converter.

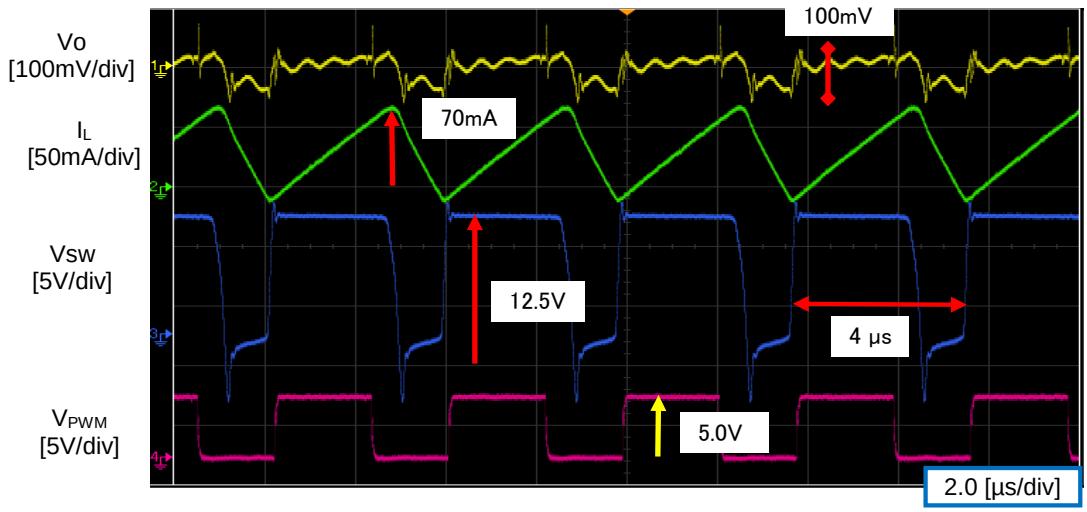


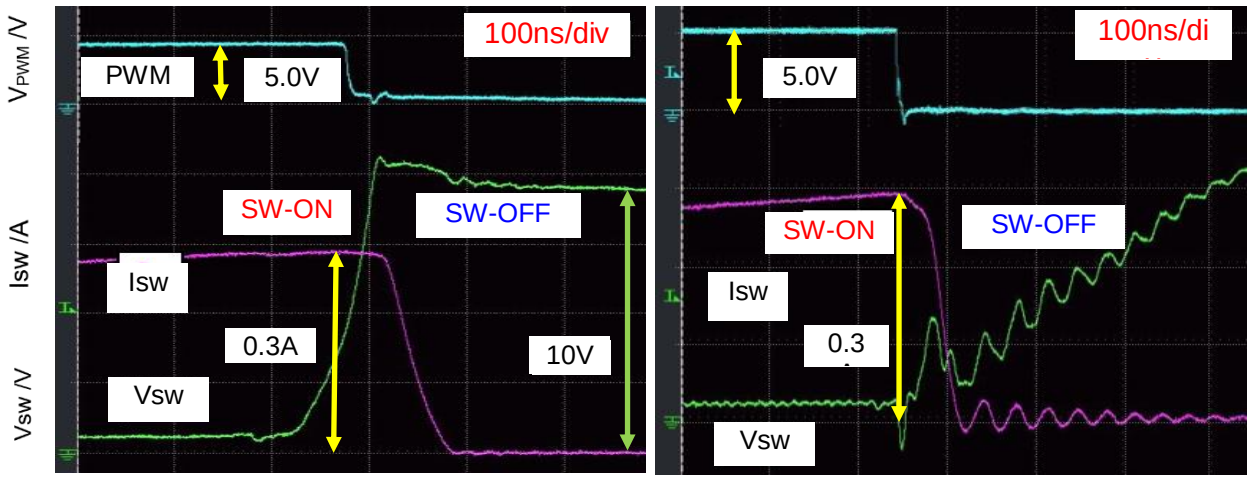
Fig. 21 Measured signals of ZVS-PWM converter

Table 4 Parameters of ZVS-PWM converter

Parameter	*Value*
Vin	10.0 [V]
Vo	6.0 [V]
L	1.0 [μH]
Cr	47 [nF]
Co	470 [μF]
Io	0.30 [A]

A resonant switching converter is well-known as a very small switching loss configuration. In this operation, the main switch M1 turns ON at the timing that Vin=Vsw as shown in Fig. 20, which means that the voltage across the switch M1 is zero and there is no switching loss. Of course, when M1 turns OFF, the capacitance Cr keeps the voltage Vsw=Vin. As a result, the switching losses are greatly reduced with the ZVS operation. Table 4 shows the parameters of this ZVS-PWM converter.

Fig. 22 shows the measured waveforms of the voltage across the switch Vsw and the current through the switch Isw in our experiment. Fig. 22 (a) shows ones in the normal buck converter, and Fig.22 (b) shows in this ZVS-PWM buck converter, when the switch turns OFF. In the normal converter, there is much overlapped between Vsw and Isw, which causes switching loss. However, in ZVS-PWM converter, there is no overlapping.



(a) Normal converter. (b) ZVS-PWM converter.

Fig. 22 Comparison of experimental waveforms of voltage and current of the switch.

4.2 SIDO Converter with ZVS-PWM Control

Fig. 23 shows the SIDO buck converter with the ZVS-PWM control [9] and Fig. 24 shows its simulation results of steady-state waveforms with the simulation conditions in Table 5. The SIDO converter consists of a single power stage with the resonant capacitor Cr, two sub-converters with the amplifiers and comparators and the control stage which includes two FFs and the comparator.

There the SEL signal is generated to determine whether the inductor current is supplied to Vo1 or Vo2 by comparing ΔVo1 and ΔVo2; Vo1 is selected when ΔVo1 > ΔVo2. We call this as "exclusive control." It is at the timing when the ZVS signal is detected and M1 is turned ON.

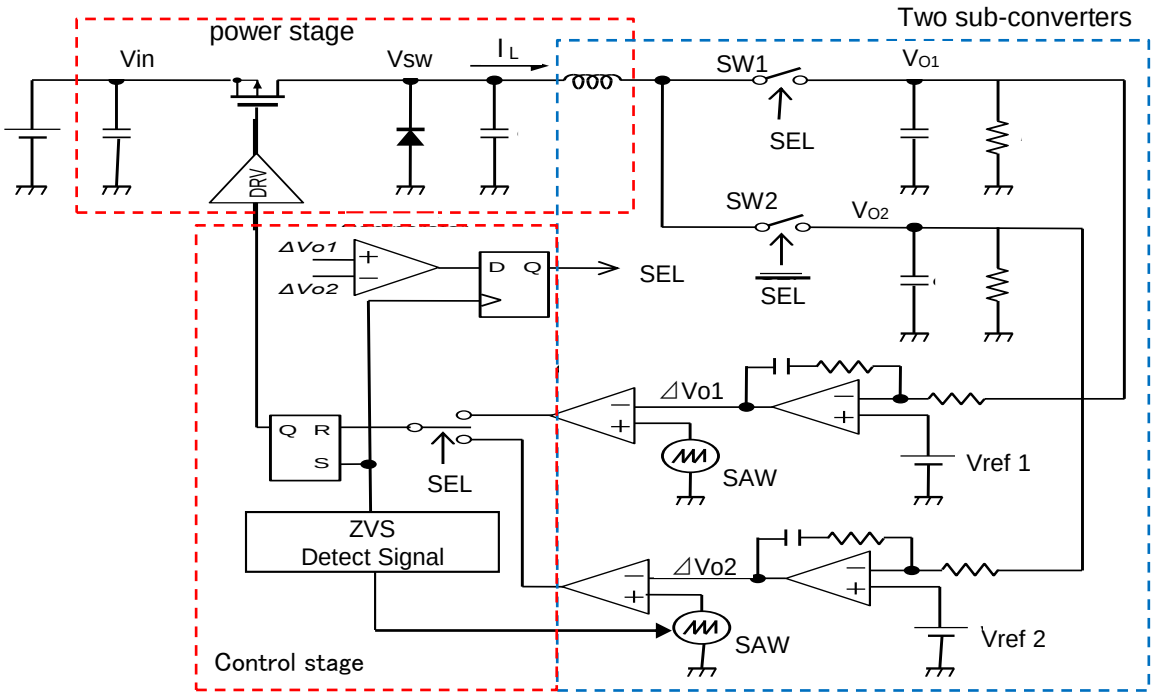


Fig. 23 SIDO ZVS-PWM converter. ZVS=Zero Voltage Switching

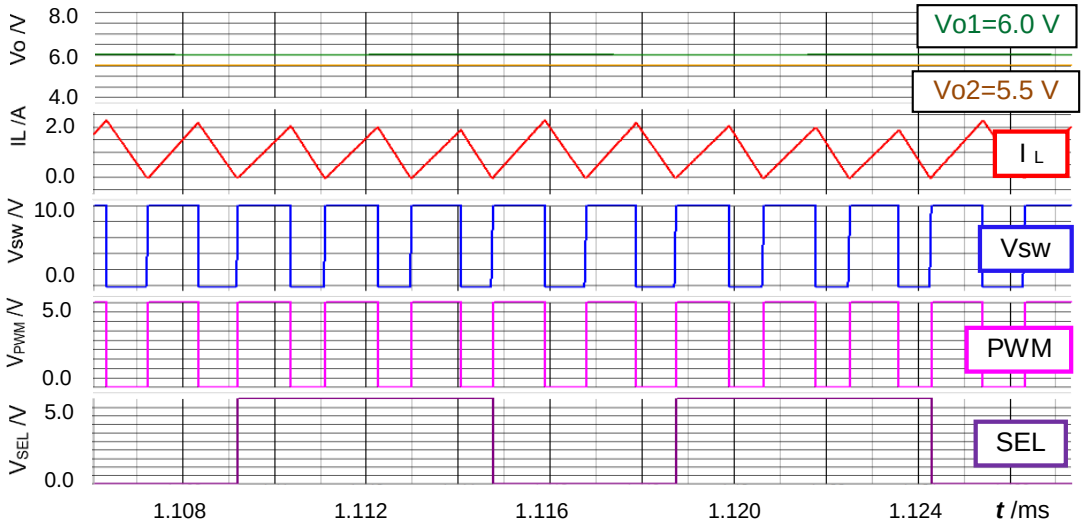


Fig. 24 Waveform of SIDO ZVS-PWM converter

Table 5 Parameters of SIDO converter

Parameter	***Value***
Vin	10.0 [V]
Vo1	6.0 [V]
Vo2	5.5 [V]
L	2.2 [μH]
Cr	1.0 [μF]
C_{O1} & C_{O2}	470 [μF]

Fig. 25 shows the transient responses of the output voltages when the load currents change with ± 0.5A in each sub-converter. The static voltage ripples of both converters are about 5mVpp at the current I1=1.0A, I2=0.5A or the vice versa. The self-regulation and the cross-regulation are in the order of several ± 15mV which is less than ± 0.3% of Vo1, Vo2. This result is satisfactory in many applications. Here, the cross-regulation means the overshoot caused by the current change of the other converter and the self-regulation means the one caused by self-current change.

In the simulation shown above, we use ideal switches for the SEL switch in each sub-converter. In the experimental circuit, there is a trouble that the MOSFET switch has the body diode inside shown in Fig. 26 (a). This trouble has appeared in other SIDO converters, and we have overcome them to replace the upside MOSFET SW1 with the diode shown in Fig.26 (b). But in this ZVS-PWM converter, it is another problem to do so because the reverse current flows from the capacitor Co1 to the resonant capacitor Cr when the sub-converter 1 is selected.

It is not so difficult to solve this problem. The solution is that the reverse current to the resonant capacitor Cr is always supplied from the capacitor Co2 in the sub-converter 2 when the sub-converter 1 is selected shown in Fig. 26 (b). In this case, the voltage V2 is set lower than V1. Fig. 27 shows the simulated waveforms of Fig. 26 (b). The yellow arrows show the period of reverse current and in which the SW2 is ON. Fig. 28 shows the measured output voltages and some signals. The output ripples are about 40mv including the spike noises.

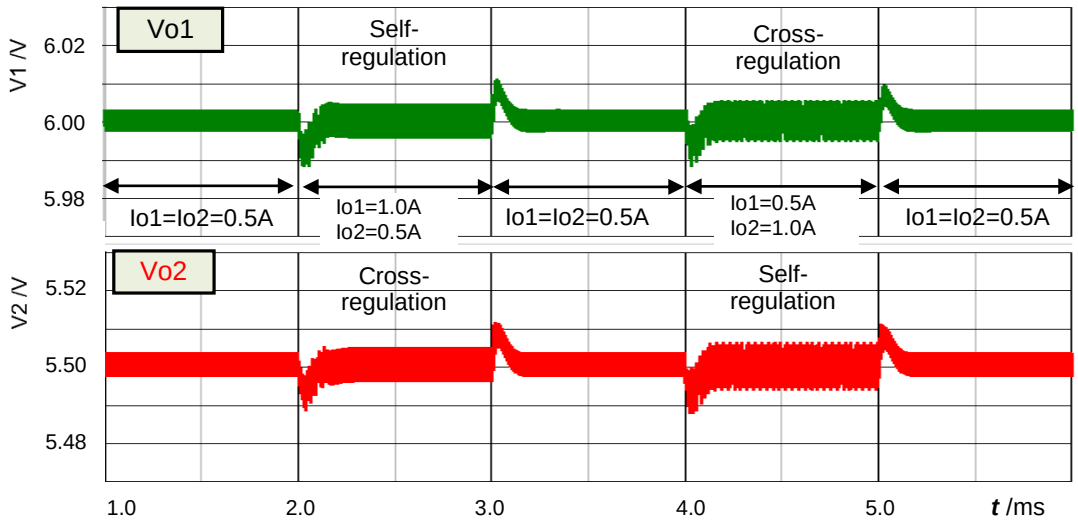
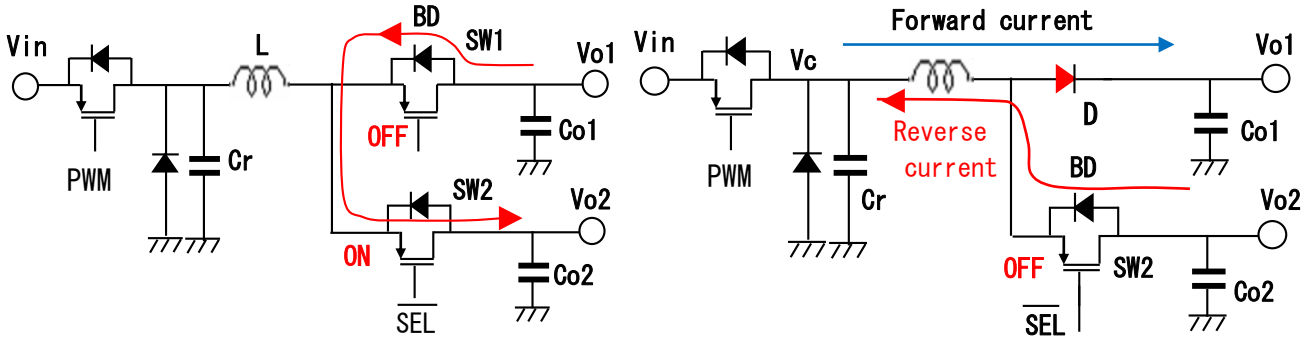


Fig. 25 Step response of SIDO converter.



(a) Problem of SIDO converter. (b) Solution when converter V1 is selected.

Fig. 26 Circuit Improvement for SIDO ZVS-PWM converter with remedy for reverse current. BD=Body Diode

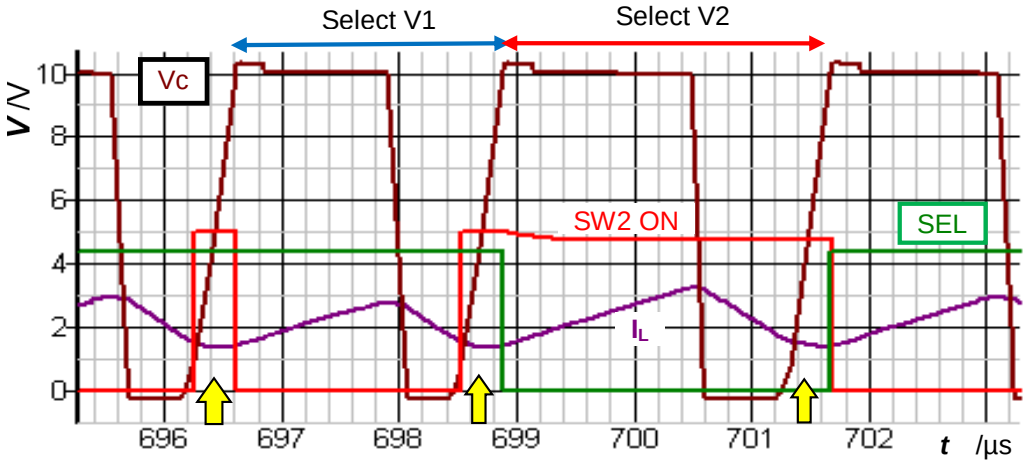


Fig. 27 Simulation result of improved circuit.

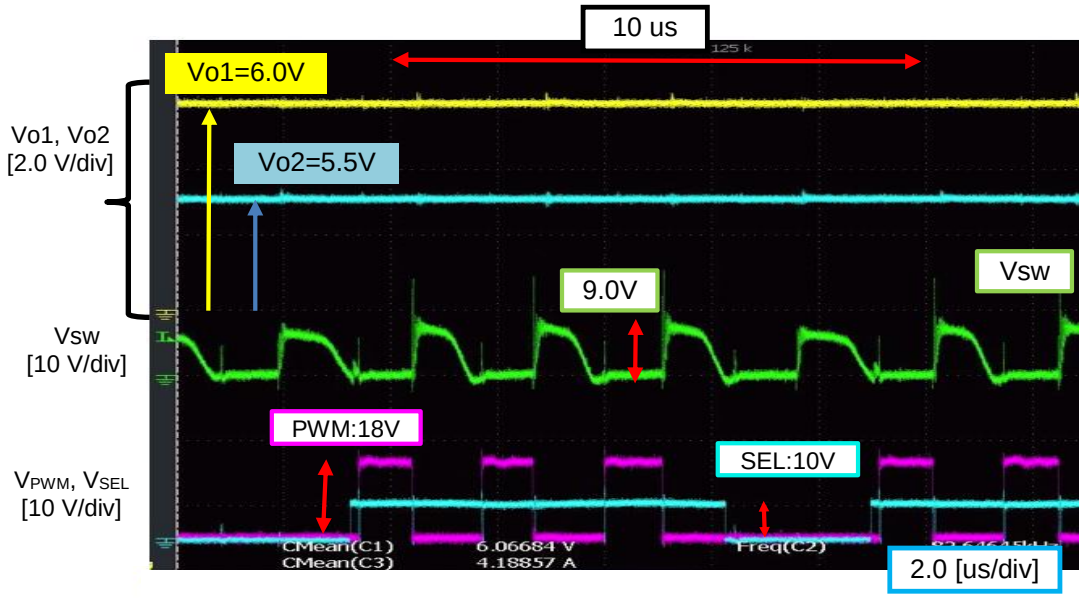


Fig. 28 Experimental results SIDO converter.

5. Soft-Switching SIDO Converter with Voltage Resonance

5.1 Basic Soft-Switching Converter with Half-Wave Voltage

Fig. 29 shows the basic soft-switching converter with half-wave voltage resonance. It consists of the power stage, the control part and the load resistor. The power stage consists of the main switch SW including the body diode Db, the main inductance Lo, the capacitance Co, the free-wheel diode Do and the resonant inductance Lr and the capacitor Cr. The control part consists of the saw-tooth generator, the voltage error amplifier and the two comparators. The comparator 1 generates the PWM signal by comparing the amplified error voltage and the saw-tooth signal SAW. The other comparator 2 compares the resonant voltage Vr and the diode voltage Vd checking the voltage across the main switch SW to generate the trigger pulse to generate the SAW signal.

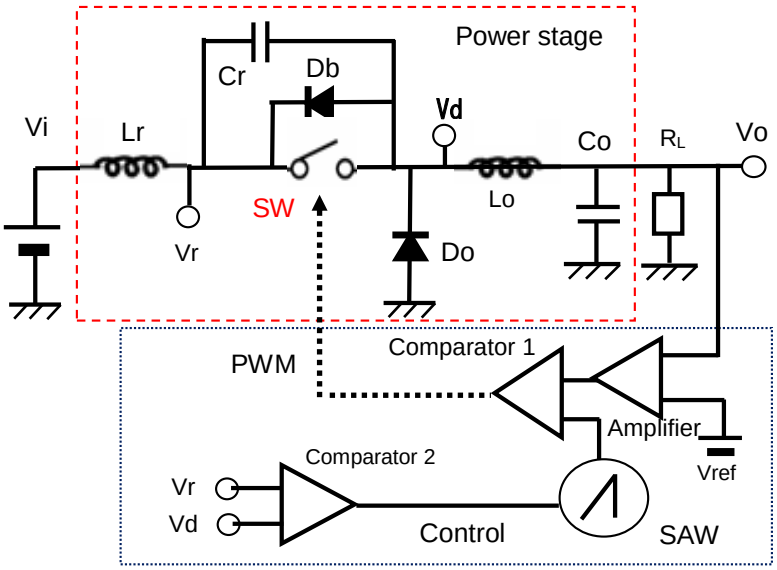


Fig. 29 Basic soft-switching converter with half-wave resonance.

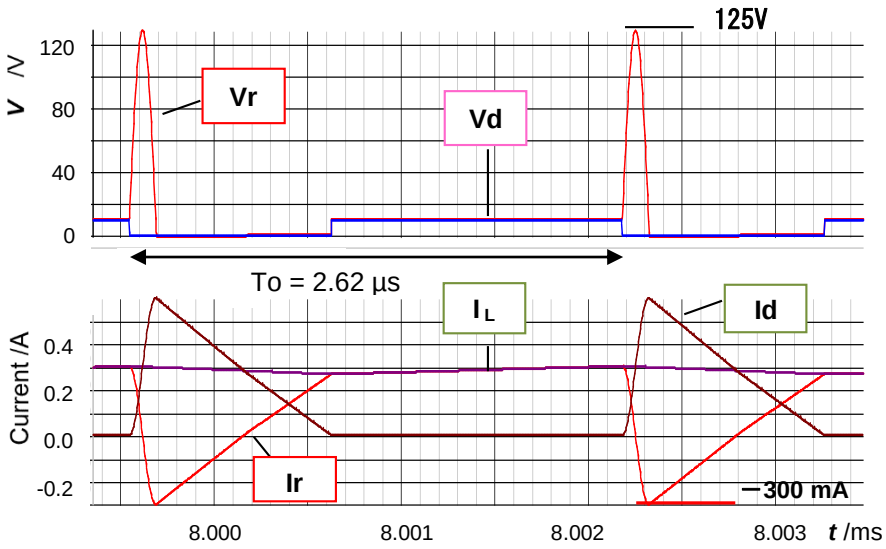


Fig. 30 Signals of half-wave resonant converter.

5.2 Simulation Results of Half-Wave Voltage Resonant Converter

Fig. 30 shows the waveforms of the basic soft-switching converter with half-wave resonance. Table 6 shows the parameters of the circuit shown in Fig. 29. The operation of the circuit is as follows:

State 1: When the main switch SW turns OFF, the resonant inductor Lr and the Cr start to resonate. The resonant voltage Vr starts to increase and reach the peak voltage which is high (about 125V) and decreases. In this state, the current of the inductor Lo flows through the free-wheel diode Do.

State 2: Vr goes down to reach Vd and the body diode Vb turns ON; then the resonance stops. The output of the comparator 2 turns high and the trigger pulse is supplied to the SAW generator. The SAW is reset to start, and the PWM turns low to make the SW ON. In this case, the SW turns ON when the voltage across the SW is 0V; this means Zero Voltage Switching (ZVS).

State 3: When the resonance stops, the current Ir of Lr flows in the reverse direction, that means from the node Vd to the input Vi gradually shown in Fig. 30. This reverse current Ir, which is supplied from the free-wheel diode Do, has the peak, and thereafter Ir decreases to 0A.

Stage 4: After Ir=0A, Ir continues increasing in the forward direction because the voltage across the Lr is about Vi. Ir goes up to reach the output current Io and the Do is cut off and the voltage Vd goes up to Vi. The output voltage Vo also increases with the increase of the current through Lo.

Stage 5: When Vo reaches the reference voltage Vref, the PWM turns low and the SW turns OFF. Then the operation returns to State 1.

The amplitude of the voltage of the resonance Vr(t) is shown in Eq. (5-1) and the condition and the resonant peak voltage must be larger than the input voltage Vi shown in Eq. (5-3).

$$Vr(t)=Vi+(Io\cdot Zr)\cdot\sin\omega t \tag{5-1}$$

$$\text{Here, } \omega=1/\sqrt{(Lr\cdot Cr)},\quad Zr=\sqrt{(Lr/Cr)} \tag{5-2}$$

$$\text{The resonant condition is: } Vr<0 \quad \therefore\ Io\cdot Zr>Vi \tag{5-3}$$

The characteristics of the soft-switching converters are as follows:

1) The resonant peak voltage Vp is very high and it depends on Io and Zr shown in Eq. (5-1).

2) The operation period is not stable because of no clock usage.

3) To keep resonant when Io=0A, the dummy current I_{dum} is needed. It is better to make I_{dum} small to get the high efficiency. It is better to set I_{dum} large to make the circuit design easy and to reduce the peak voltage.

Table 6 Parameters of soft-switching converter

Parameter	***Value***
Vi	10 [V]
Vo	5.0 [V]
Io	0.25 [A]
Lr	20 [μH]
Cr	100 [pF]
Lo	50 [μH]
Co	220 [μF]

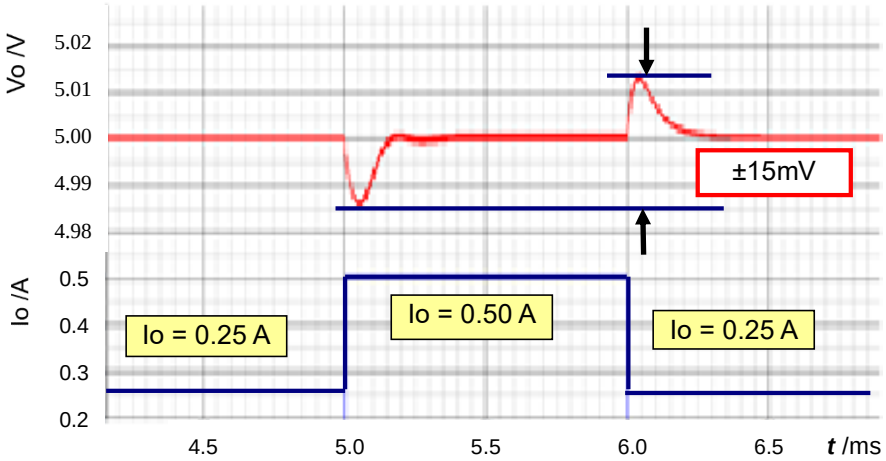


Fig. 31 Step response with half-wave resonance.

Fig. 31 shows the output voltage ripple Vo and the step response with current step Δ0.25A. The static ripple is less than 2mVpp at Io=0.5A and the over/under-shoot is about 15mV with the current step ΔI=0.25A. The settling time is about 0.2ms shown in Fig. 31. The operating frequency is about 380 kHz.

5.3 Basic Full-wave Voltage Resonant Converter

Fig. 32 shows the soft-switching converter with the full-wave voltage resonance. The difference of the circuit from the half-wave voltage resonance converter is only the diode inserted before the SW in series. Fig. 33 shows the waveform of the full-wave voltage resonance converter in Fig. 32. See that the resonant voltage Vr has the positive and negative voltage peaks. The waveform of Vr starts from Vi through the positive peak and the negative peak to end at the voltage of Vd which is about 0V. The operation of this circuit is similar to the half-wave resonant converter. The PWM signal turns Hi when the resonant voltage Vr comes back to about 0V from the negative resonant voltage shown in Fig. 33. In this circuit, Io is 0.9A and the resonant peak voltage goes very high of 400V. The parameters are the same as Table 6 and the operating frequency is about 1.25 MHz.

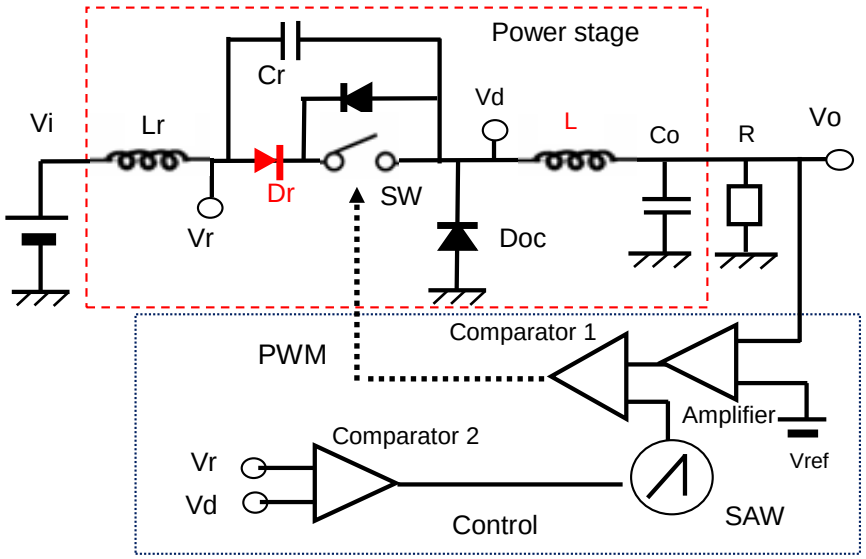


Fig. 32 Basic soft-switching converter with full-wave resonance.

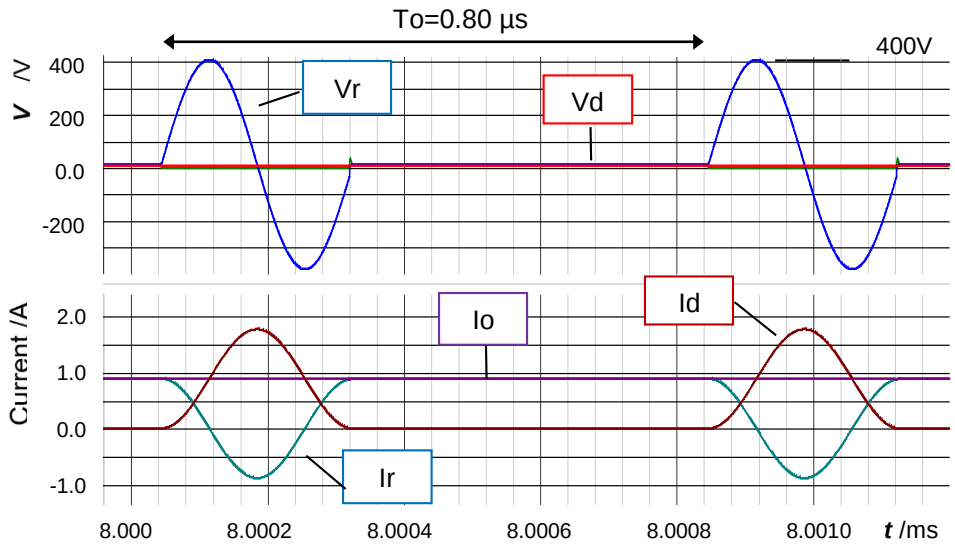


Fig. 33 Signals of full-wave resonant converter.

5.4 SIDO Soft-Switching Converter with Half-Wave Voltage

Fig. 34 shows the SIDO soft-switching converter with the half-wave voltage resonance. It consists of the power stage, two sub-converters and the control part. The control part consists of the comparator 1, the selector, the comparator 2 which generates the PWM signal and the comparator 3 which supplies the trigger pulse to the SAW signal generator. The SEL signal and the PWM signal are generated with the exclusive method to operate like as the SIDO buck converter shown in Fig. 3.

Fig. 35 shows the waveforms of the SIDO soft-switching converter, here V1=5.0V, V2=4.0V, I1=0.50A and I2=0.25A, respectively. The sub-converter 1 is selected when the SEL signal is high. The period of each cycle is different from each other and the peak level of the inductor current I_L is variable from 750mA to 830mA, whose average is about 700mA. The peak level of the resonant voltage Vr is almost constant of 55V. The operation period is variable from 3.5μs to 7.0μs. Fig. 36 shows the output voltage ripples, which are less than 5mVpp when I1=0.50A and I2=0.25A. The maximum ripple is about 10mVpp when I1=0.75A and I2=0.25A. The over/under-shoots are about 5mV at the current step ΔIo=0.25A.

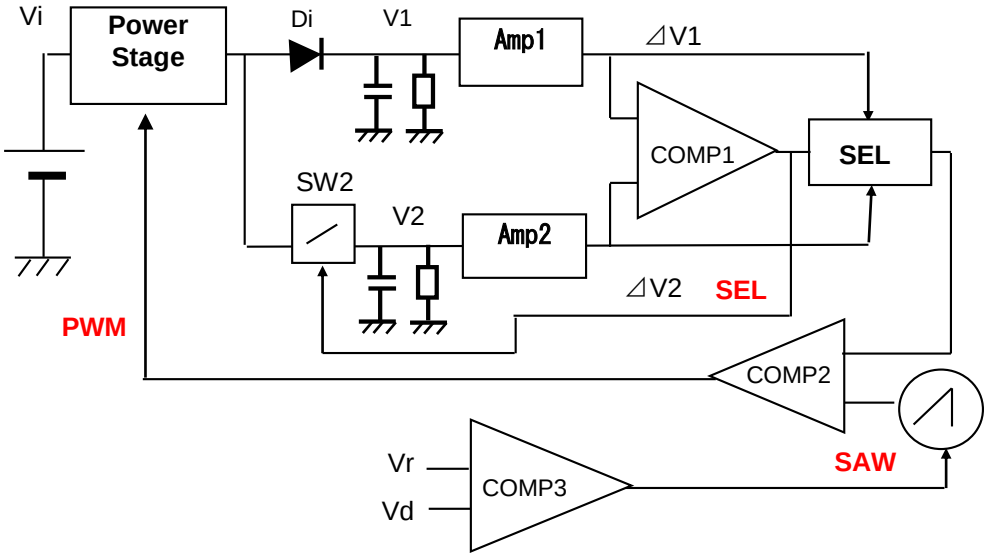


Fig. 34 SIDO soft-switching converter. Amp=Amplifier, COMP=Compartor

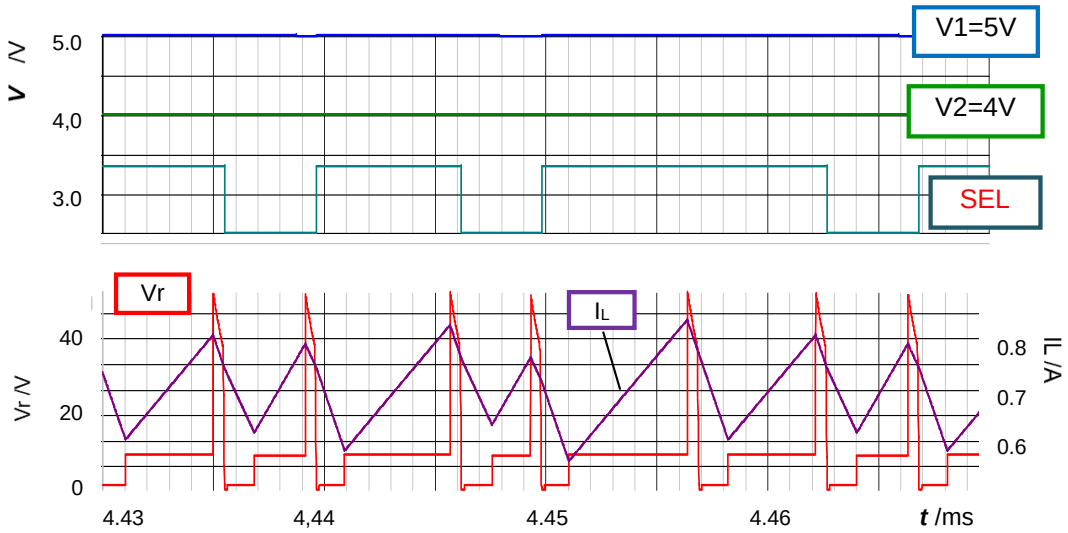


Fig. 35 Waveforms of SIDO converter.

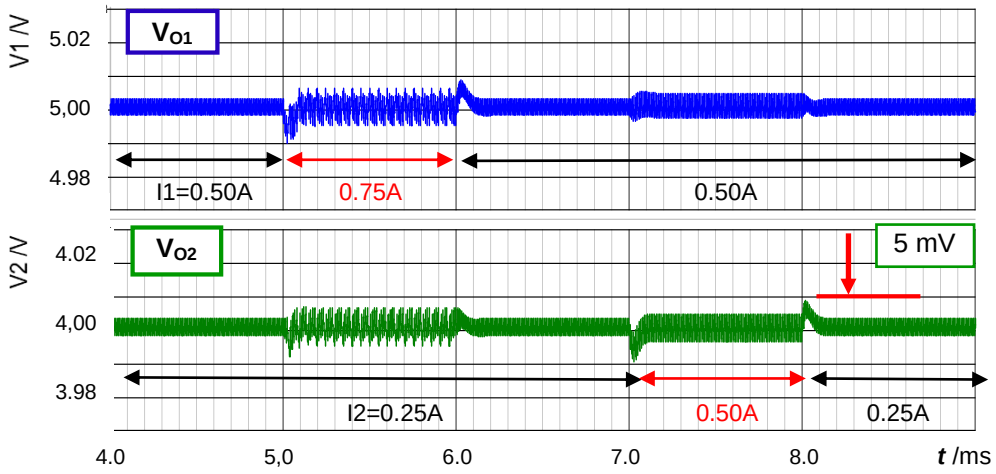


Fig. 36 Output ripples of SIDO converter.

6. Current-mode Controlled SIDO Converter

6.1 Basic PWM Converter with Current-mode Control

The basic switching converters usually operate with the PWM voltage-mode control. By adding the current-mode control to the voltage-mode control, the step response with an output current step is greatly improved, thanks to direct detection of the inductor current change. Fig. 37 shows the buck converter with current-mode control. It consists of the power and control stages. In the power stage, there are the inductor current detector, the slope compensator and two adders. In the current-mode controlled converter, the slope compensation has to be used not to be resonant, when the duty ratio of the PWM signal is larger than 50%.

Table 7 shows the parameters of the converter with the current-mode control. Here, Ac means the sensitivity of the current detector and Gc means the gain of the amplifier 2 Amp2 in Fig. 37. Fig. 38 shows the output voltage ripple Vo and the output current Io. The ripple is less than 2mVpp at Io=1.0A and the over/under-shoot is ±6mV at the current step ΔIo=±0.5A. Fig. 39 shows the signals of the current-mode control. Here Vac means the current detected voltage with slope compensation.

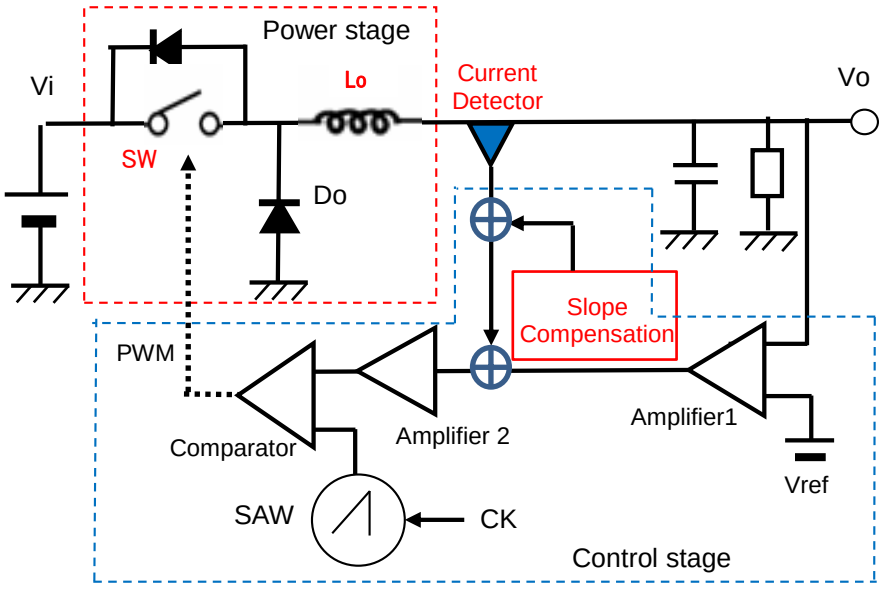


Fig. 37 Converter with current-mode control.

Table 7 Parameters of current-mode converter

Parameter	***Value***
Vi	12 [V]
Vo	3.3 [V]
Io	0.5/1.0 [A]
Lo	10 [μH]
Co	470 [pF]
Ac	2.0 [V/A]
Gc	× 5

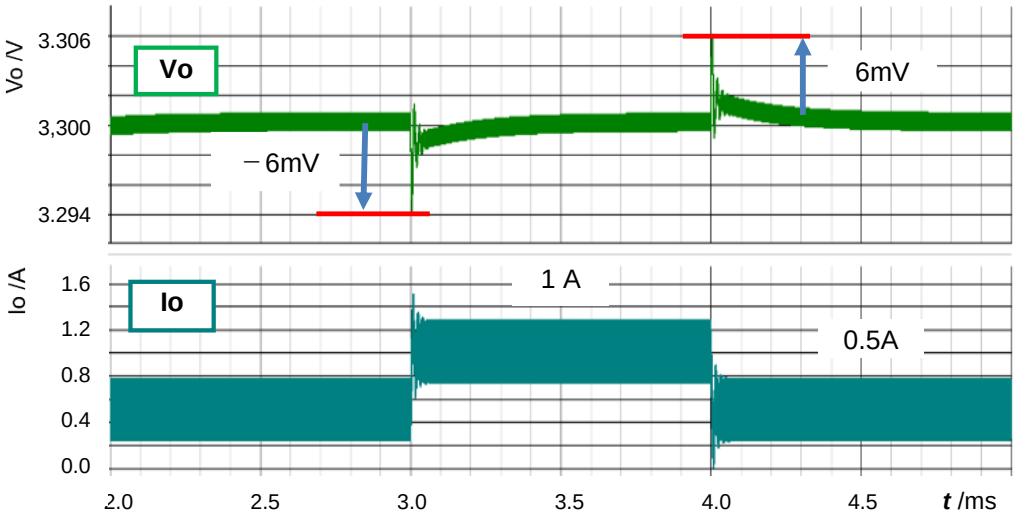


Fig. 38 Ripple of current-mode converter.

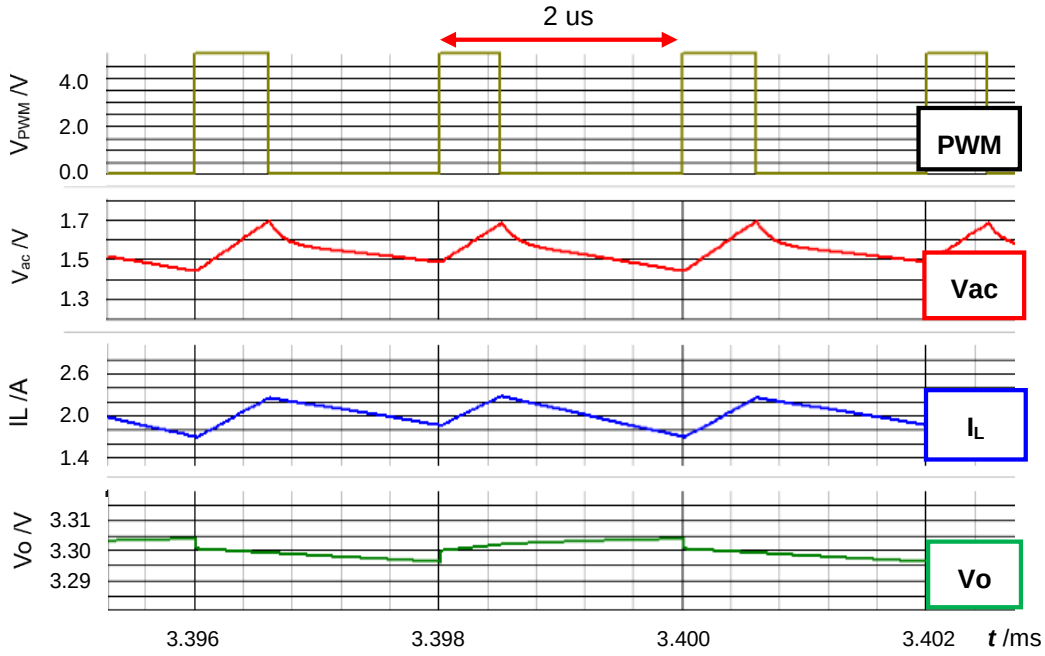


Fig. 39 Signals of current-mode converter.

6.2 SIDO Converter with Current-mode Control

Fig. 40 shows the SIDO converter with current-mode control. It consists of the power stage, the control stage and two output stages including the error amplifiers of the output voltage. In the normal SIDO converter, each converter usually includes the current detector of its inductor current and the slope compensation circuit. This converter has the single current detector and the single slope compensation circuit. The single current detector is set in series of the inductor with the slope compensation. The outputs of the dual converters are selected at the selector which chooses one of the amplified error voltages, ΔV1 or ΔV2. The select signal SEL is generated at the comparator Comp1 which compares ΔV1 with ΔV2. The output ripples are stable with unification of the current detector and the slope compensation.

Fig. 41 shows the output voltage changes where the total current Io increases from 2A to 8A. The ripples of V1 and V2 increase with 8mVpp to 32mVpp. Note that the output ripple level is proportional to the output current Io. To reduce the ripple, it is better to make the value of the inductor and the capacitor larger. The under-shoot is less than 20 mV at the total current step ΔIo=2A.

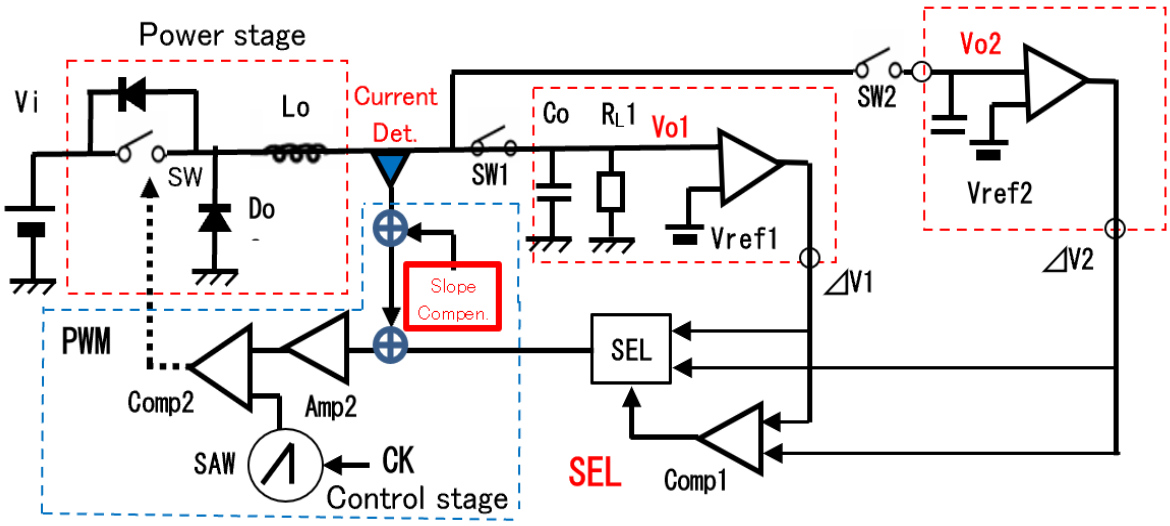


Fig. 40 SIDO converter with current-mode control. Det.=Detector

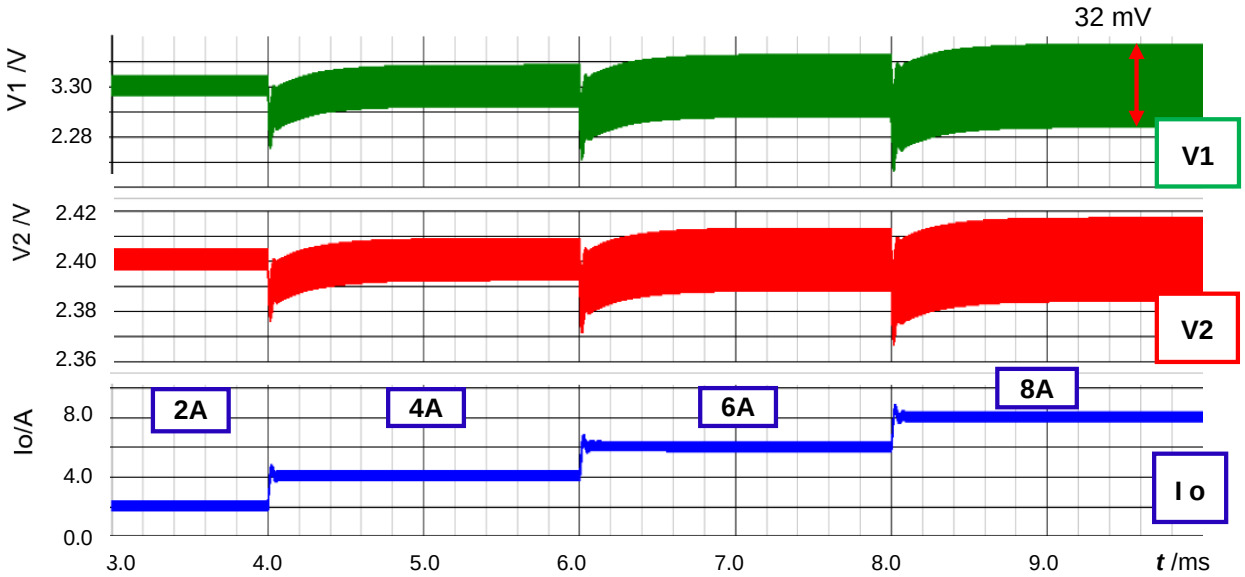


Fig. 41 Output ripples of SIDO converter with current-mode control.

7. Single-Inductor Multi-Output (SIMO) Buck Converter with Four Outputs

7.1 Single-Inductor Four-Output Buck Converter

Fig. 42 shows the SIMO buck converter with the power stage and the four sub-converters [8]. These sub-converters are plug-in type connected to the power stage. Each sub-converter includes usual output capacitor, an OP-amplifier, a reference voltage source Vr and the additional parts, which are an input select diode, a select switch, a comparator1 for generating PWM pulse, a comparator2 for generating select signal, and a latch. Each sub-converter supplies an error voltage ⊿Vo and the PWM pulse. The main switch in the power stage is controlled by the PWMo pulse which is the sum of each PWM. Fig. 43 shows the circuit for generating the common maximum voltage Vcom from each ⊿Vo. The voltage Vcom is supplied to each sub-converter to generate the select signal SEL which controls the switch in the self-converter.

In order to decide the sub-converter controlled in next period, the wired OR circuit shown in Fig. 43 is used, which supplies the maximum error voltage V_{dv} to each comparator in each sub-converter. For example, when ΔV1 is the highest voltage in all voltage ΔV1 ~ΔV4, the voltage of the OR node V_{dv} is ΔV1-V_{sel}. Here, V_{sel} is the voltage across the selected diode. In this case, R1 is much larger than R2 to set the voltage V_{com} lower than V_{sdv}. Hence SEL1 comes high and the switch in the sub-converter turns ON.

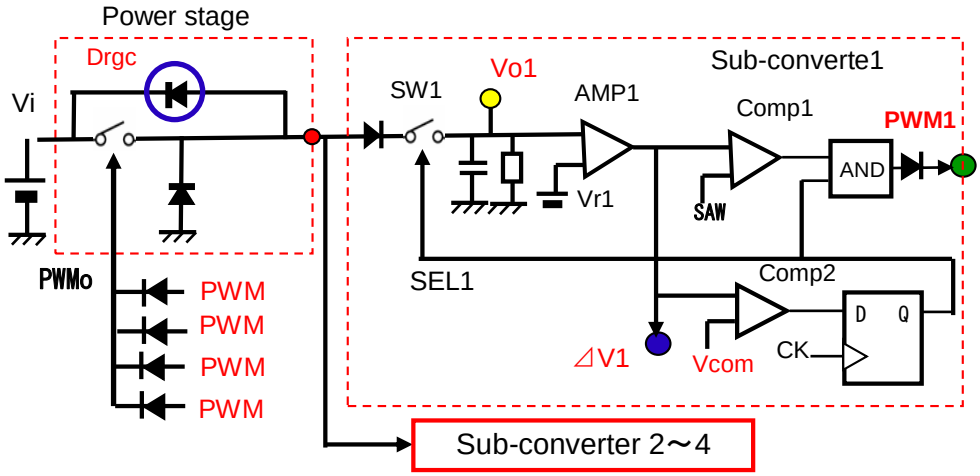


Fig. 42 SIMO buck converter with four sub-converters.

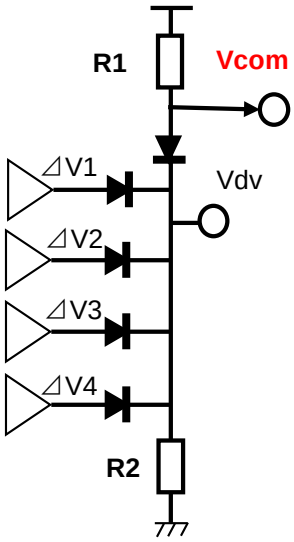


Fig. 43 Control stage.

7.2 Simulation Results of SIMO Converter

Fig. 44 shows the simulation results of the SIMO converter with four output voltages, V_1～V_4. Here, the static current of each sub-converter is 0.5A and the current change ΔIo of I1 or I4 is 0.5A each. In this converter, only one select signal is chosen by the control circuit shown in Fig. 45. When every output voltage of each sub-converter is higher than each reference voltage, all select signals SEL1 ~ SEL4 are low, and any switch in each sub-converter is not selected. This case is shown in Fig. 45 and there is no SEL signal with star marks. In this case, the regenerated current Ir in the inductor flows to the voltage source through the diode across the voltage source and the output Vo marked with blue circle.

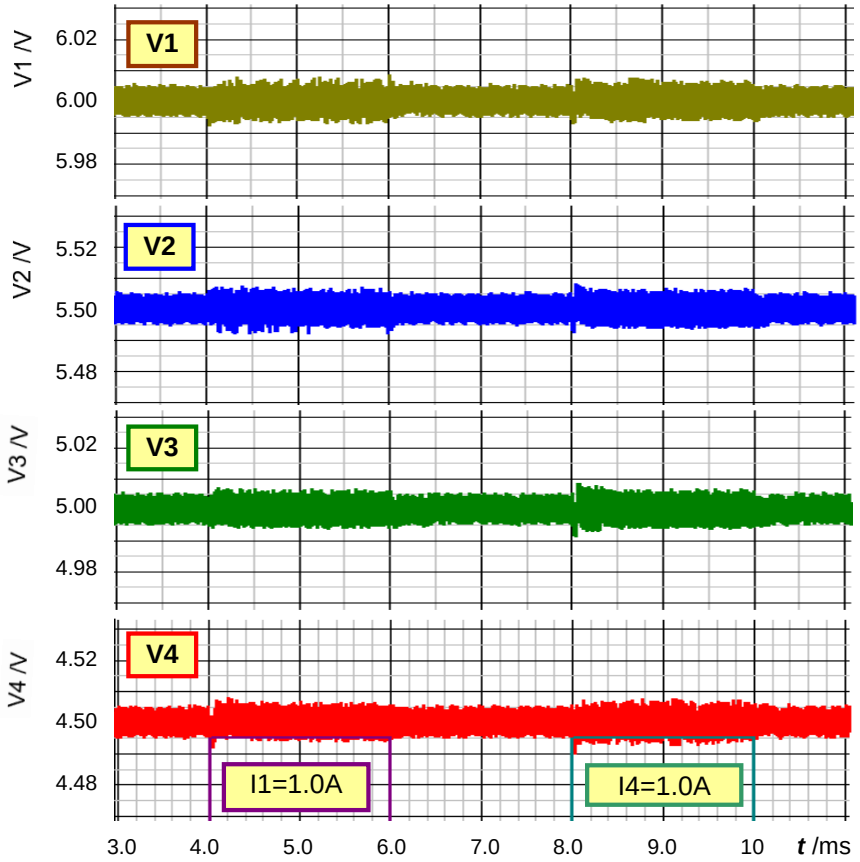


Fig. 44 Simulation results of SIMO converter.

Table 8 Parameters of SIMO converter

Parameter	***Value***
Vin	10.0 [V]
V_1	6.0 [V]
V_2	5.5 [V]
V_3	5.0 [V]
V_4	4.5 [V]
Io	0.5 [A] each
L	0.2 [μH]
C	470 [μF] each
Fck	500 [kHz]

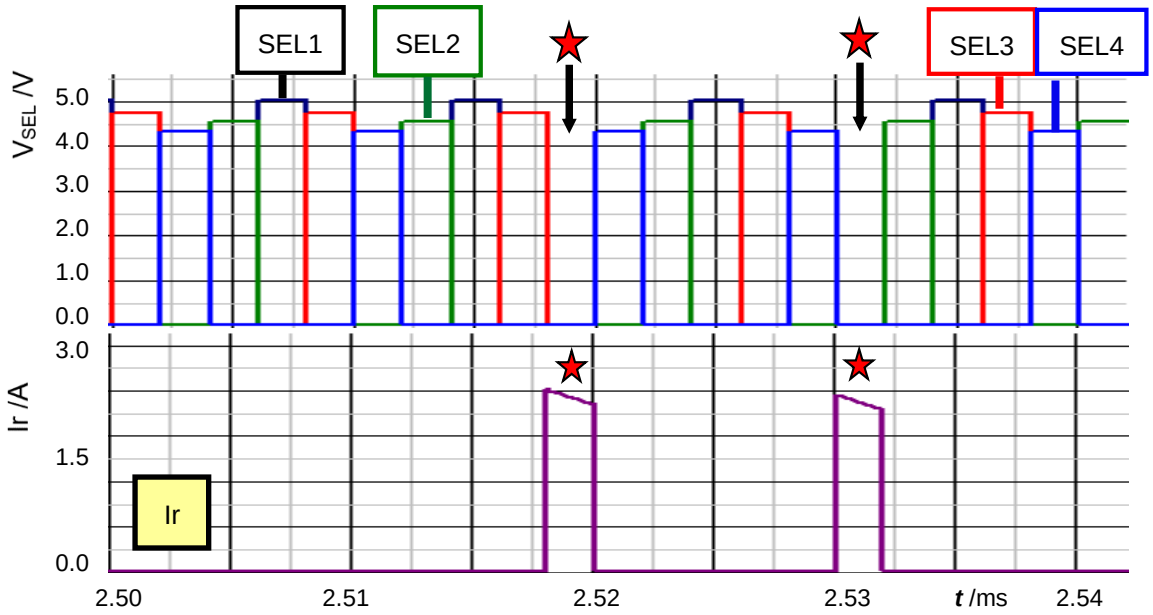


Fig. 45 Waveforms of SIMO converter.

8. Conclusion

This paper has proposed the technology to realize the SIDO buck type switching converters with PWM, hysteretic, ZVS-PWM, soft-switching or current-mode control with the exclusive control method. The SIDO converters can reduce the number of the inductors and make the converter size small. These converters consist of a power stage with a single inductor and two sub-converters. To realize the SIDO converters, the exclusive control is utilized to supply the energy from the power stage to the sub-converter whose error voltage is larger than the other.

In the SIDO converter with the hysteretic control, the CR circuit to generate the triangular signal is connected to the output of the sub-converter 1 because the voltage of the tail edge of the inductor is changed with the change of the SEL signal. In the SIDO converter with the ZVS-PWM control, the reverse current charging the resonant capacitor Cr is always supplied from the sub-converter 2. In the SIDO converter with soft-switching control, it is the problem that the resonant peak voltage gets high when the load current is large. In the SIDO converter with the current-mode control, the current detector and the slope compensation circuit is unified to make the control system stable. In the SIMO converter with four outputs, the regenerated current in the inductor flows to the voltage source through the diode connected to the tailing edge of the inductor, when any sub-converter is not selected.

Control power supplies should be used properly depending on the purpose of use. The PWM control SIDO power supply is applied for a circuit with a relatively small load change (less than 50%). The ripple control power supply is applied for circuits with large load change. For circuits where EMI noise such as unnecessary radiation or conducted noise is a problem, simple ZVS-PWM controlled converter or half-wave / full-wave type resonant soft switching converter is applied. In this case, note that the resonant voltage of these resonant converter depends on the load current and reaches 100 V or more. In recent years, the current-mode controlled converter tends to be mainstream, and it is expected that SIDO converters of this method will prevail in the future.

When the load current difference is greatly large, the duty ratio of the SEL signal largely changes. At this time, the output voltage ripple becomes very large in proportion. Countermeasures to this problem are the future issues of the SIDO technology.

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