Journal of Technology and Social Science (JTSS)

EMI Reduction in Switching Converters With Pseudo Random Analog Noise

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Keywords: switching converter, EMI reduction, spread spectrum, M-sequence, pseudo analog noise, PLL circuit, clock frequency modulation

Abstract: This paper proposes an EMI reduction method by extending spectrum spread using a PLL circuit and frequency modulation of a clock pulse with pseudo analog noise generated by a modified M-sequence circuit. The PLL circuit makes the reference clock to be modulated with non-periodic analog noise supplied from the 3-bit M-sequence circuit. Extended pseudo analog noise is produced by inverting and/or exhanging (swapping) 3-bit signals. Using this modified clock supplied from the PLL circuit for the saw-tooth signal in the switching converter, the spectrum of the PWM pulse is widely spread, and the peak levels of the spectrums of the fundamental frequency and the harmonic frequencies are substantially reduced.

1. Introduction

In recent years, the expansion of the mobile device usage has been accelerated by the progress in our information society [1,2]. The switching power converter is well-known and widely used for its small size, light weight and high efficiency. There the Pulse Width Modulation (PWM) control method is usually used. However, electromagnetic noise concentrates at specific frequencies of the PWM signal and its higher harmonics, which causes an Electro Magnetic Interference (EMI) problem. Since the standards for EMI are getting strict along with the spread of electronic equipment, the reduction of the electromagnetic noise in the switching converter is very important [1-8].

The conventional methods for EMI noise suppression are a shield plate for unnecessary noise and/or a low-pass filter (LPF) in an input power line for conductive noise. These suppression methods are very costly and bulky, so that an essential noise suppression method has been desired. It is well-known that the white noise (or thermal noise) is very effective to modulate the clock frequency in order to reduce the EMI noise peak [3,4]. Unfortunately, it is difficult to generate a white noise at low cost with the analog circuit. In the contrast, the conventional digital spread spectrum method [1,2] is to use only discrete digital spread and has a limit to the noise reduction unless a lot of digital hardware with high frequency clock operation is used; this method is suitable for digital controlled power supply circuits.

This paper proposes a new method in order to reduce the EMI noise using a spread spectrum technique by adding fluctuation to the PWM signal to modulate the PWM signal phase. The proposed method uses an M-sequence circuit based on primitive polynomials to generate a digital pseudo random noise, which is fed to a following analog LPF to produce a pseudo random analog noise; this is provided to a phase-locked loop (PLL) with very slow response so that the PLL output clock frequency is modulated randomly without a period and its spectrum peaks are reduced significantly.

Notice that spread spectrum clock generators (SSCGs) for digital processors often handle clocks higher than several hundred MHz so that they required sophisticated PLL circuits. However, there only several MHz clocks are managed so that their circuit design difficulty is relaxed.

2. Spread Spectrum Methodology in Switching Converter

2.1 Switching converter with PWM control: Basic configuration

Fig. 1 shows the buck type switching converter and Fig. 2 shows its associated waveforms. In the power stage, the main switch SW is controlled ON/OFF by the PWM pulse which is supplied from the control stage. When the SW is ON, the current through the inductor Lo increases and flows from the voltage source Vin through the SW to the output capacitor Co and the load resistor R_L. When the SW is OFF, the inductor current flows through the diode and decreases as shown in Fig. 2.

In the control stage, the amplifier compares and amplifies the difference between the output voltage Vo and the reference voltage Vref. The amplified voltage ⊿Vo is compared with the saw-tooth signal SAW to generate the PWM pulse which controls the SW. The SAW signal is generated at the saw-tooth generator which is triggered by the clock.

In this converter, the voltage of the diode is steeply switched from Vin to 0V or vice versa, and the inductor current quickly changes its flow through the SW or the diode. These changes of the voltage or the current cause large unnecessary radiation noise and conductive noise, which occurs in the power line from the source Vin; these are called the EMI noises which spread to the harmonic frequencies. The maximum allowable EMI level is regulated by law.

Fig.3 shows the spectrum of the PWM pulse and Fig. 4 shows the conductive noise spectrum. In these spectrums, many line spectrums appear at the fundamental clock frequency and its many harmonics. Usually the peak power level at the clock frequency is higher than any other harmonics, as shown in Fig. 3 and Fig. 4.

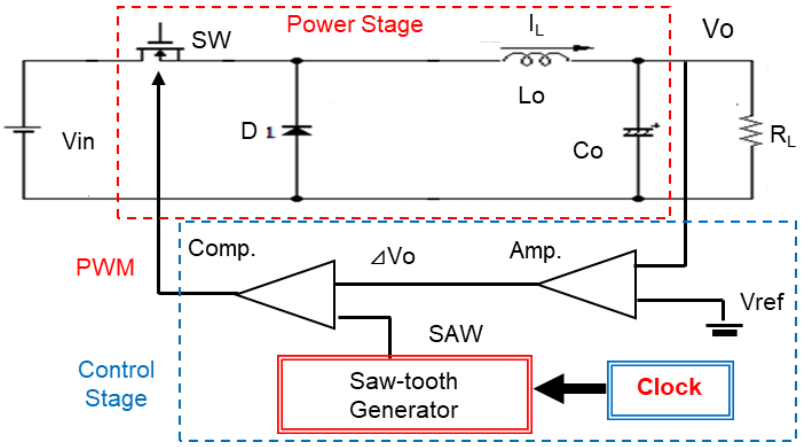


Fig. 1 Buck converter with PWM control.

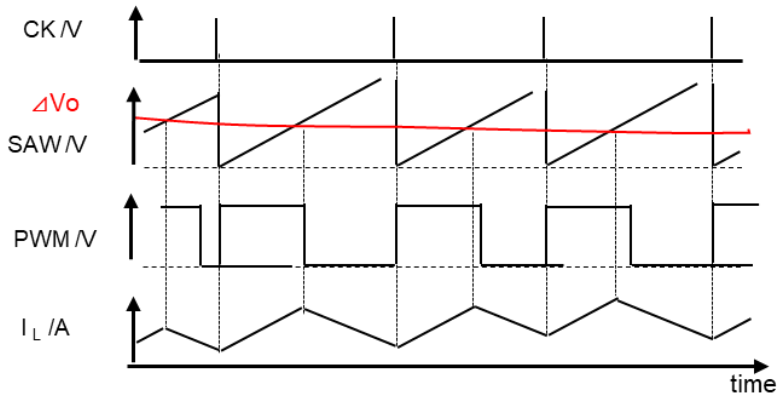


Fig. 2 Illustrated signals of switching buck converter.

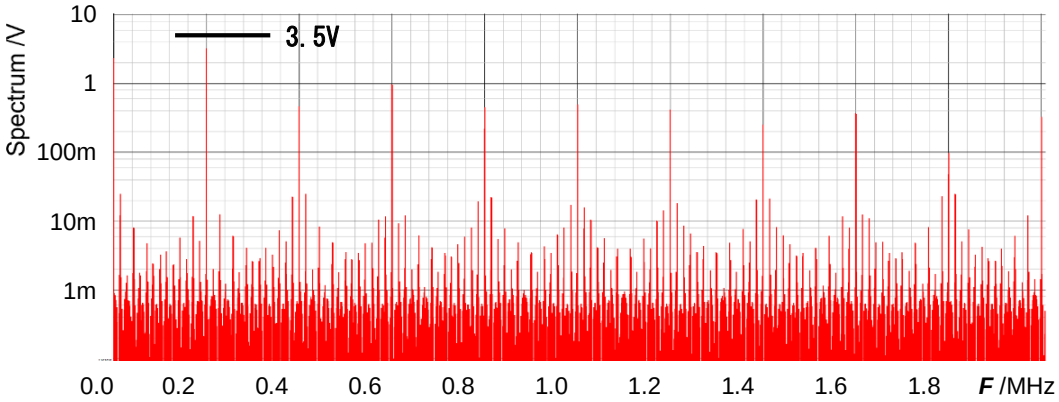


Fig. 3 Spectrum of PWM pulse.

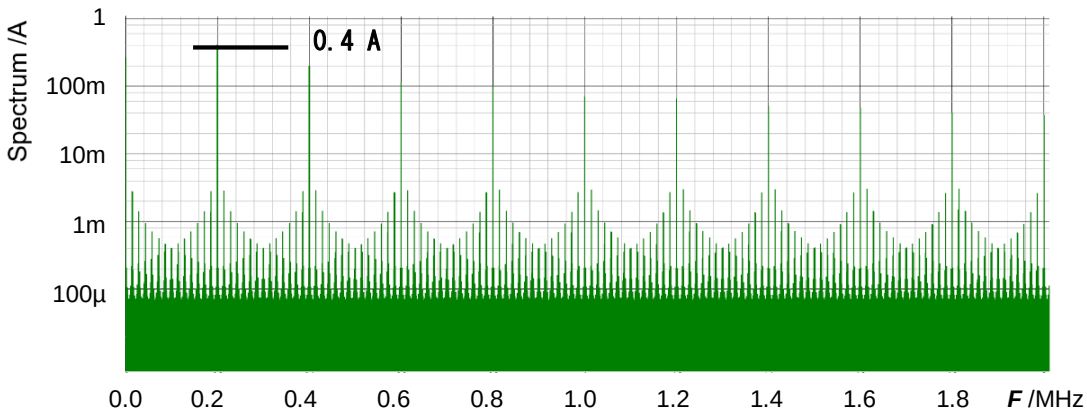


Fig. 4 Spectrum of conductive noise.

2.2 Spread spectrum with modulation of clock pulse

It is well-known that the frequency or phase modulation of the clock pulse in the switching converters reduces the EMI noise of the PWM pulse; this means that the peak level at the clock frequency in the spread spectrum is decreased. Fig. 5 shows the conventional clock modulation circuit in the control stage of the switching converter and Fig. 6 shows the timing chart of the modulated clock generator. The difference of the control stage circuit in Fig. 5 from the one in Fig. 1 is only the addition of the modulator to the clock generator, so that the SAW signal phase is modulated s shown in Fig. 6.

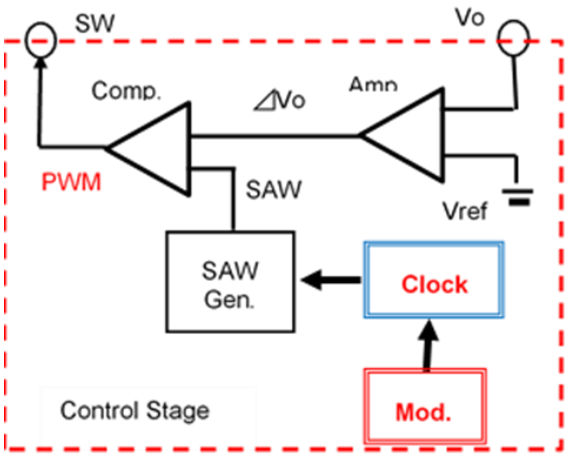


Fig. 5 Clock modulator in control stage.

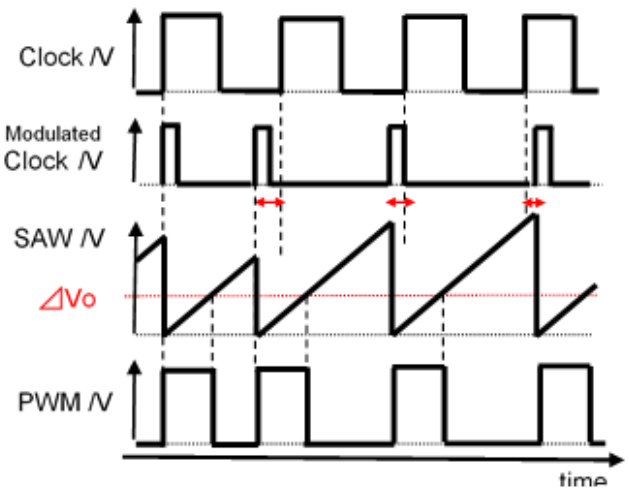
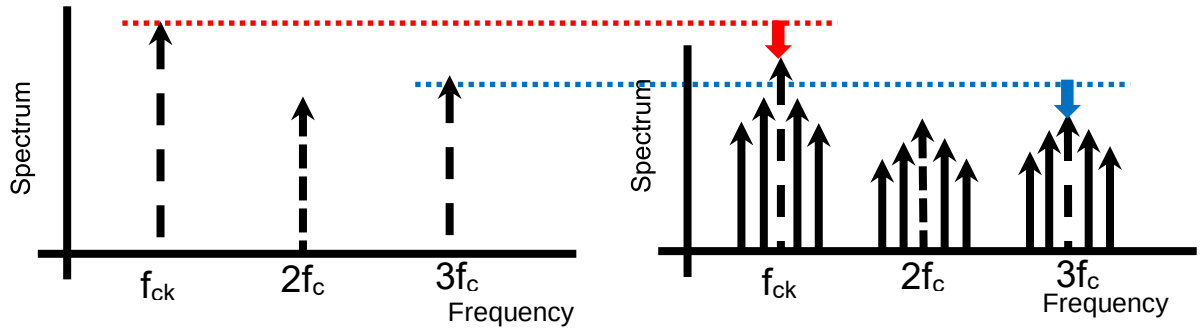


Fig. 6 Illustrated signals of modulated signals.

Fig. 7 (a) shows the spectrum of the PWM pulse when the clock is not modulated, whereas Fig. 7 (b) shows the spectrum when the clock is modulated. The energy of the clock noise is spread to around of the clock frequency spectrum as shown in Fig. 7, which is the conceptual explanation of the spread spectrum of the phase modulation. There appear several line spectrums shown by the real arrows spread discretely in both sides of the fundamental frequency spectrum shown by the dashed arrows and its harmonics; we see that the levels of the fundamental spectrum shown by the dashed arrows are reduced with the phase modulation.



(a) Non-modulated spectrum. (b) Modulated spectrum.

Fig. 7 Conceptual explanation of spread spectrum of PWM pulse

2.3 Conventional digital phase modulation of clock pulse

Fig. 8 shows the block diagram of the conventional digital phase modulation for the control stage in Fig. 5. It consists of the shift registers, the pulse selector and the random code generator. The number of the shift clock during one period needs more than 256, which is generated with the same number of Flip-Flops in the shift register. The original clock is delayed little by little as shown in Fig. 9 and there are generated 256 phase shifted clocks. One of these shifted clocks is selected during a single clock period using the pulse selectors controlled by 8-bit random code from the generator. Here, in order to reduce the EMI noise, the random phase modulated clock has to be used to generate the SAW signal.

In the digital modulation circuit in Fig. 8, it needs a large amount of the digital circuit in case of 256-shift clock. It needs the 256-step shift register and the 256-bit selector which consists of 256 8bit-input AND gates and a 256-input OR gate, that are relatively large digital circuits. Moreover, the frequency of the shift clock is 10 times of the main clock. Usually the frequency of the main clock is 200k ~ 500kHz, then the frequency of the shift clock will be higher than 200MHz. It is too high frequency for the analog LSI fabricated with mature process. In this sense, this digital modulation method is suitable for a digital controlled switching converter.

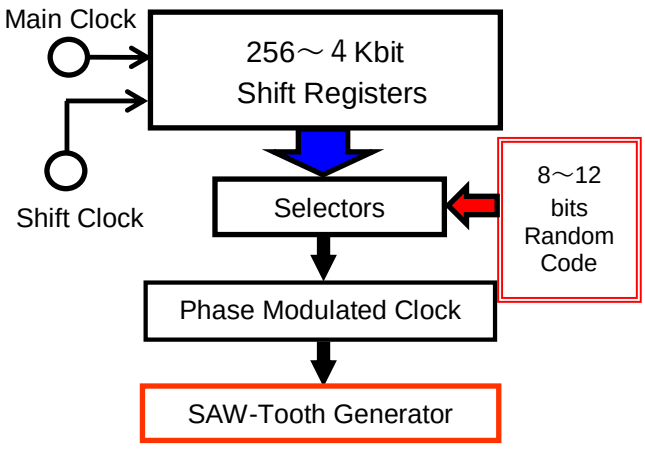


Fig. 8 Block diagram of digital modulation.

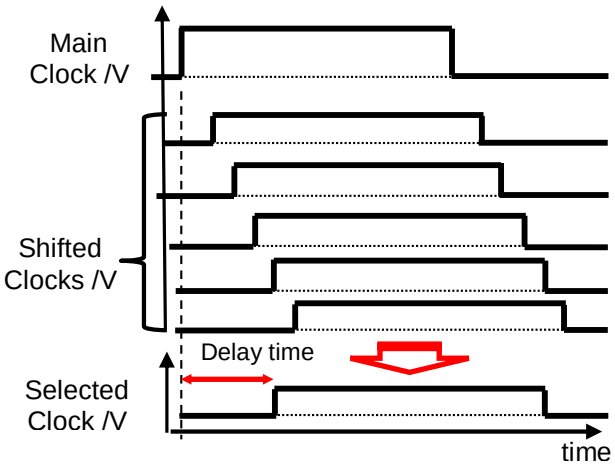


Fig. 9 Timing chart of modulated clocks.

3. Novel Clock Modulation with Pseudo Analog Noise

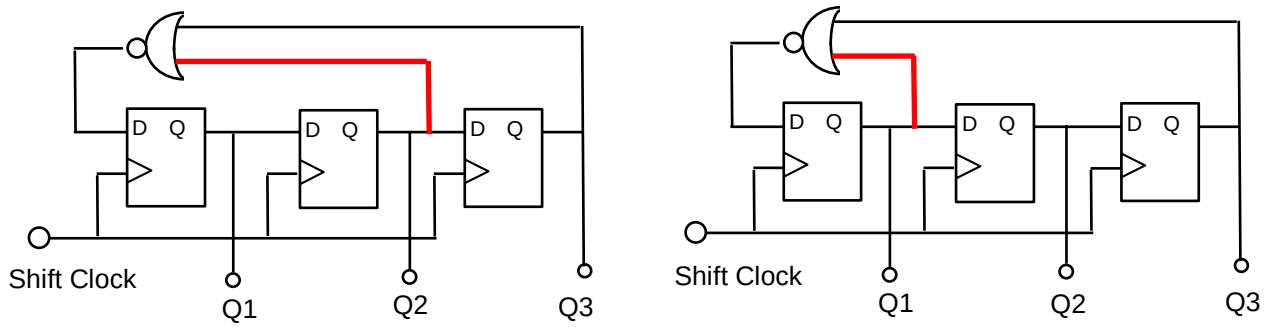
3.1 Pseudo analog noise with PLL clock generator

M-sequence circuit using the primitive polynomial is known as a method to generate random digital noise. Fig. 10 shows the M-sequence circuits of 3-bit expressed in Eq. (3-1) and (3-2). Each is composed of 3-bit shift-registers and Exclusive NOR (Ex-NOR) gates. Depending on Eq. (3-1), the outputs of 3rd and 2nd bits are connected to the Ex-NOR gate inputs and its output is supplied to the D-input of the 1st Flip-Flop. It generates N=(2^n -1) levels when the number of the shift register bits is n (or the dimension of the primitive polynomial is n). The number of levels is 7 at n=3 and there are two primitive polynomials as below.

Fig. 11 shows the output analog levels converted from binary codes (Q3, Q2, Q1) in Fig. 10 by M-sequence circuit based on two equations. There are cyclic patterns of 7 levels with 0-1-3-6-5-2-4 or 0-1-2-5-3-6-4. These analog patterns are deformed to the smooth signal, which we call a pseudo analog noise; however, this smooth noise is still cyclic signal. If we observe the signal for just a short period of time, no signal patterns will be found. However, if we observe it longer, we recognize that the similar signal patterns occur repeatedly. In order to add more fluctuation, the pseudo analog noise is provided to Phase Locked Loop (PLL) circuit. Then, the PLL circuit output is modulated by the variation of the added pseudo analog noise voltage. Moreover, the PLL is not locked with the input noise because of its dull characteristics of the step response shown in Fig. 13; in this case, the PLL circuit output is the frequency modulated clock.

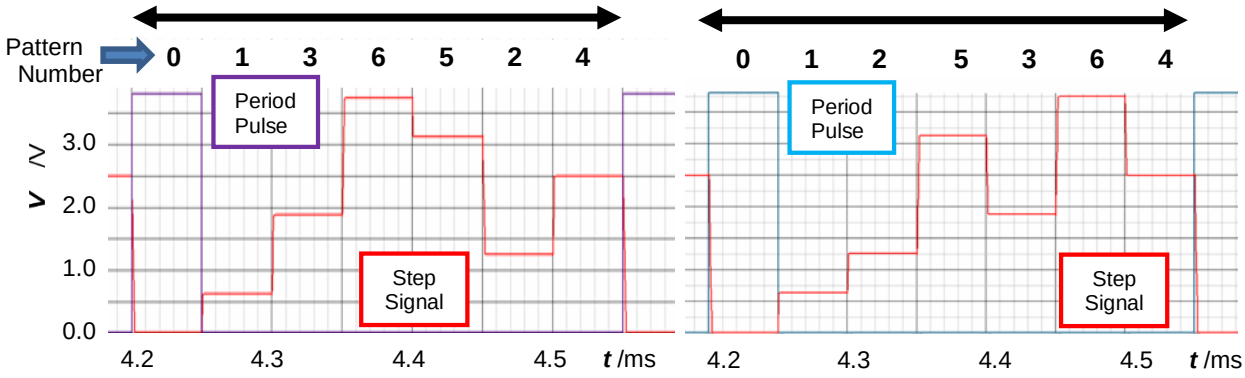
$$G(x) = x^3 + x^2 + 1 \quad (3\text{-}1)$$

$$G(x) = x^3 + x + 1 \quad (3\text{-}2)$$



(a) Circuit of Eq. (3-1). (b) Circuit of Eq. (3-2).

Fig. 10 M-sequence circuits of two primitive polynomials.



(a) Waveforms with Eq. (3-1). (b) Waveforms with Eq. (3-2).

Fig. 11 Waveforms of output levels with M-sequence circuits.

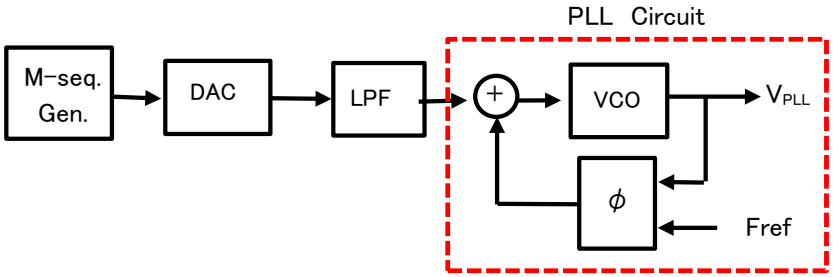


Fig. 12 Block diagram of analog modulation.

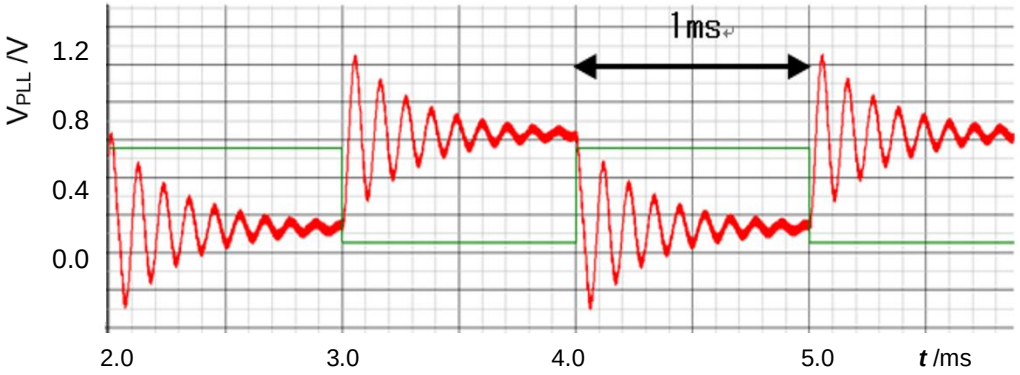


Fig. 13 Characteristics of the PLL circuit.

3.2 Simulation results of spread spectrum with pseudo analog noise

The circuit of the DC-DC switching buck converter with the control stage is shown in Fig. 1. The clock generator with the modulation circuit and the pseudo analog noise generator are shown in Fig. 5 and Fig. 12. Table 1 shows the parameters of the switching converter. Fig. 14 shows the pseudo noise Vn, the PLL control signal V_{cont} and the output voltage ripple ⊿Vo using Eq. (3-1). Here, Vn is periodic, but V_{cot} or ⊿Vo is non-periodic. The frequency of the clock pulse is 400 kHz and the shift clock for the M-sequence in Fig. 10 is 10 kHz, so that the periodic frequency of Vn is 1.43 kHz. The output ripple ⊿Vo is about 10mVpp. This simulation uses the circuit simulator (SIMPLIS).

Fig. 15 shows the spectrums of the PWM signal (red) and the conductive noise (green). Fig. 15 (a) shows the spectrums without the pseudo analog noise Np and Fig. 15 (b) shows those with Np. The peak level of the fundamental clock (400 kHz) is reduced from 3.0V to 0.55V, which is 14.7 dB reduction. The level of the harmonic frequency (1.2 MHz) is from 1.0V to 0.1V (-20 dB). The peak level of the conductive noise is reduced from 350mV to 70mV (-14 dB).

Table 1 Parameters of the converter

Parameter	***Value***
Vin	10.0 [V]
Vo	5.0 [V]
Io	0.5 [A]
L	5.0 [μH]
Co	470 [μF]
Fck	400 [kHz]

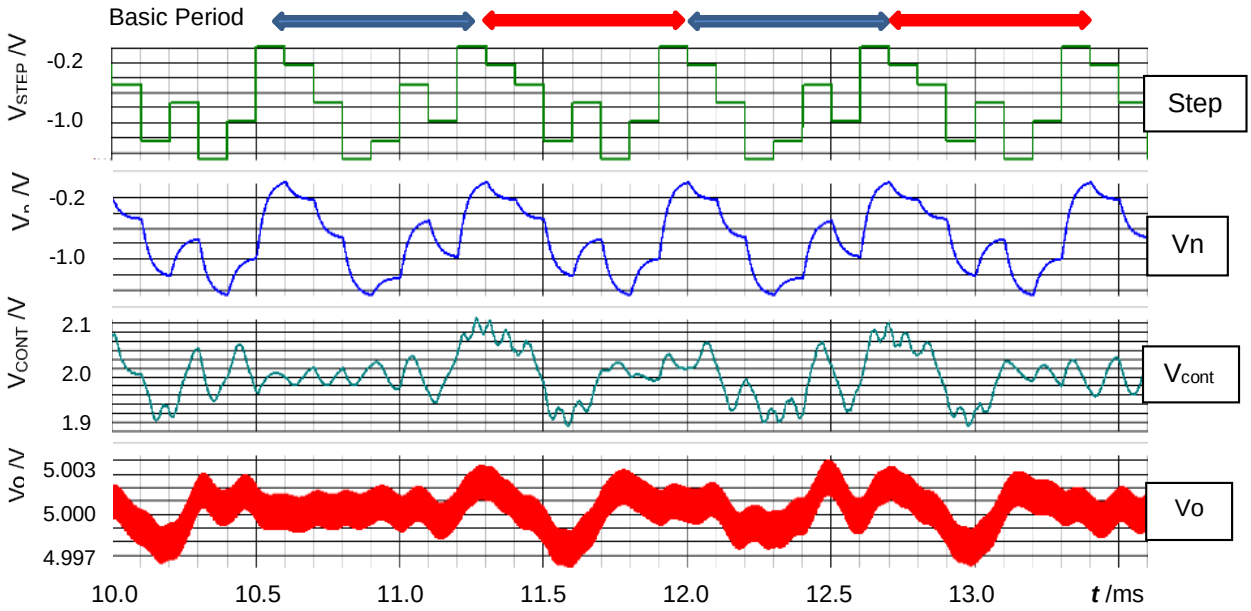
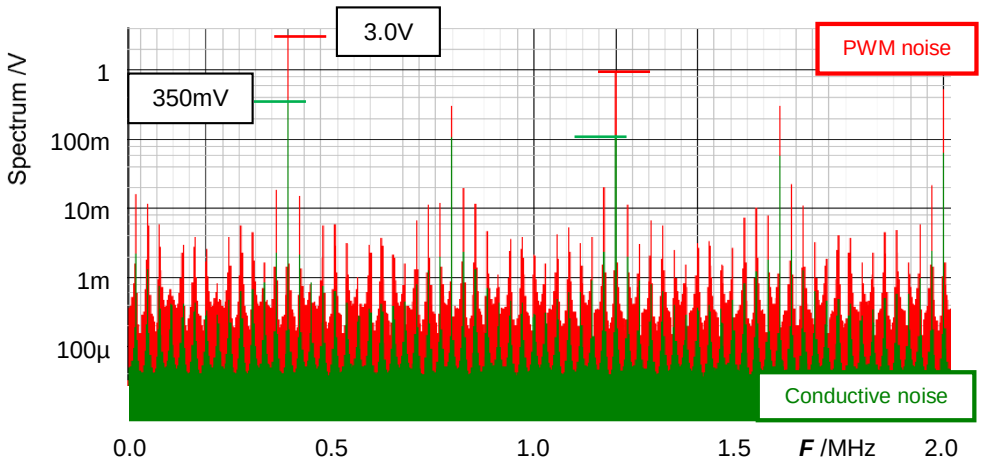
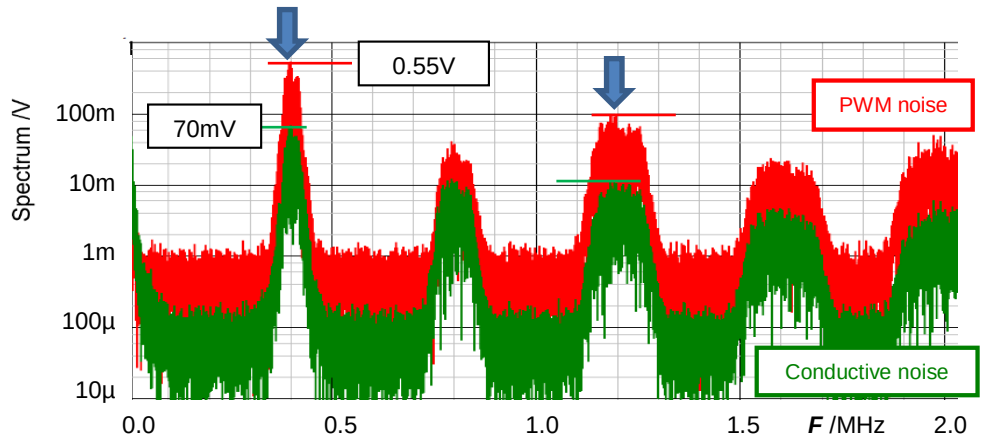


Fig. 14 Non-periodic signal of clock pulse.



(a) Spectrum without analog noise.



(b) Spectrum with analog noise.

Fig. 15 Spectrum of the PWM pulse and the conductive noise.

4. New Analog Noise Generators with Bit Operation

4.1 Expansion of analog pattern length with bit reverse

We have investigated a new analog noise generator with bit-exchange which is generated from an M-sequence circuit. The longer the pattern of the analog noise is, the lower the peak level of the fundamental frequency is and the wider the side-band spectrums of the harmonic frequencies spread. The 3-bit makes 8 analog levels and the number of permutations of the trains of the pattern level changes makes ${}_7P_7 = 7! = 5{,}040$. Here the start level is set to 0 because these trains are periodic. So there is ability to increase the number of permutations of the trains when the number of the bits is increased. By adding the other patterns generated from the combination of these pattern levels in series, we obtain double or more length pattern. For example, reversing some of the bits from the M-sequence circuit makes the new pattern levels.

The other patterns generated from the combination of these pattern levels in series are added. Equations (4-1) ~ (4-8) show the results of the bit-reversed level streams of the original equations (3-1) and (3-2). In these results, there is no identical stream and we can understand that using theses streams in the analog noise cycle makes the analog noise period longer by 8 times of the original equations. The pattern length adding the bit-reverse method makes $T_1 = 8 \cdot 2 \cdot 7 = 16 \cdot To$ patterns a period. Here To is the original pattern length of 7.

	【Based on Eq. (3-1)】		【Based on Eq. (3-2)】	
1) $Q_1Q_2Q_3$:	0 - 1 - 3 - 6 - 5 - 2 - 4 -	:	0 - 1 - 2 - 5 - 3 - 6 - 4 -	(4-1)
2) $\overline{Q_1}Q_2Q_3$:	1 - 0 - 2 - 7 - 4 - 3 - 5 -	:	1 - 0 - 3 - 4 - 2 - 7 - 3 -	(4-2)
3) $Q_1\overline{Q_2}Q_3$:	2 - 3 - 1 - 4 - 7 - 0 - 6 -	:	2 - 3 - 0 - 7 - 1 - 4 - 6 -	(4-3)
4) $\overline{Q_1}\overline{Q_2}Q_3$:	3 - 2 - 0 - 5 - 6 - 1 - 7 -	:	3 - 2 - 1 - 6 - 0 - 5 - 7 -	(4-4)
5) $Q_1Q_2\overline{Q_3}$:	4 - 5 - 7 - 2 - 1 - 6 - 0 -	:	4 - 5 - 6 - 1 - 7 - 2 - 0 -	(4-5)
6) $\overline{Q_1}Q_2\overline{Q_3}$:	5 - 4 - 6 - 3 - 0 - 7 - 1 -	:	5 - 4 - 7 - 0 - 6 - 3 - 1 -	(4-6)
7) $Q_1\overline{Q_2}\overline{Q_3}$:	6 - 7 - 5 - 0 - 3 - 4 - 2 -	:	6 - 7 - 4 - 3 - 5 - 0 - 2 -	(4-7)
8) $\overline{Q_1}\overline{Q_2}\overline{Q_3}$:	7 - 6 - 4 - 1 - 2 - 5 - 3 -	:	7 - 6 - 5 - 2 - 4 - 1 - 3 -	(4-8)

4.2 New pattern generator and simulation results with bit reverse

Fig.16 shows the simulation circuit of the new M-sequence circuit with bit-reverse based on Eq. (3-1). The bit-reverse is realized with 3 Exclusive-OR gates controlled by an additional 3-bit counter, which is triggered once an M-sequence 3-bit counter period. In Fig. 16, the additional counter counts up when all bits of the M-sequence counter are low. In this way, the output of a Digital-to-Analog Converter (DAC) connected to the additional counter is shown in Fig. 17 and its periodic length expands 8 times of To.

Fig. 18 shows the output voltage ripple ΔVo of the converter with the pseudo analog noise and Fig. 19 shows the spectrum of the PWM signal and the conductive noise with bit-reverse. The ripple is 8.5 mVpp which is non-periodic signal. The ripple level will be reduced by adjusting the inductance and capacitance values. The peak level of the fundamental clock is reduced to 500 mV (-15.6 dB) and that of the conductive noise is reduced to 60 mV (-15.3 dB). The effect of the EMI reduction is little with only bit-reverse.

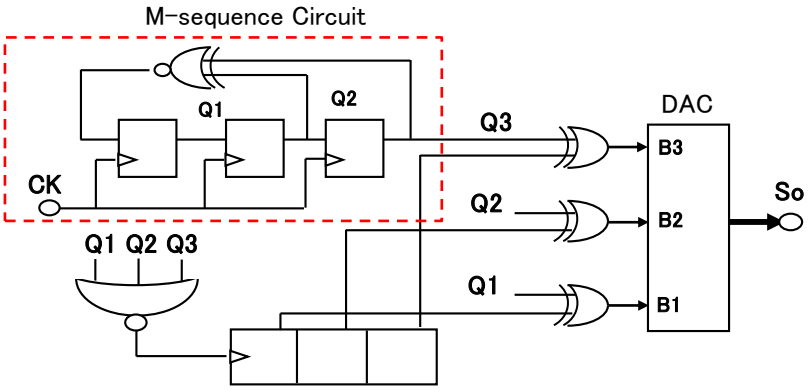


Fig. 16 Pattern generator with bit-reverse.

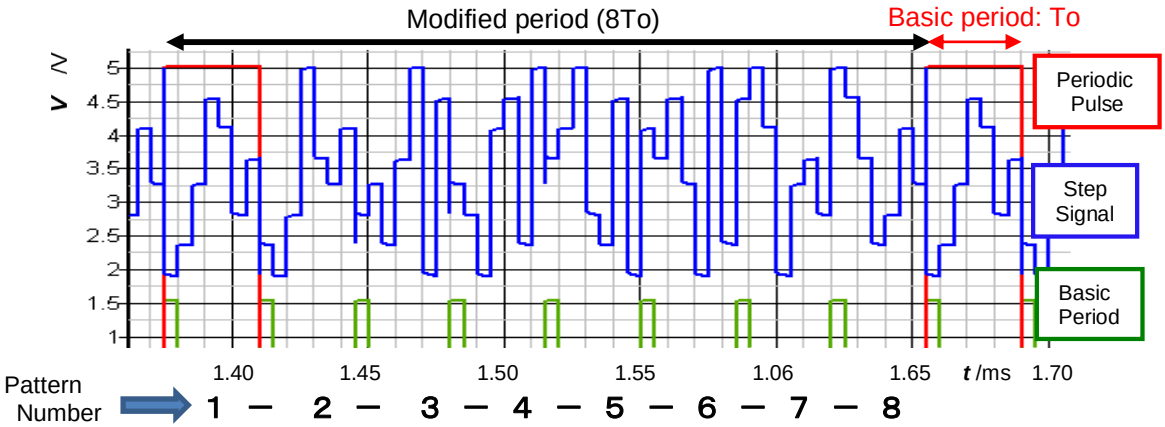


Fig. 17 Expanded pattern with bit-reverse.

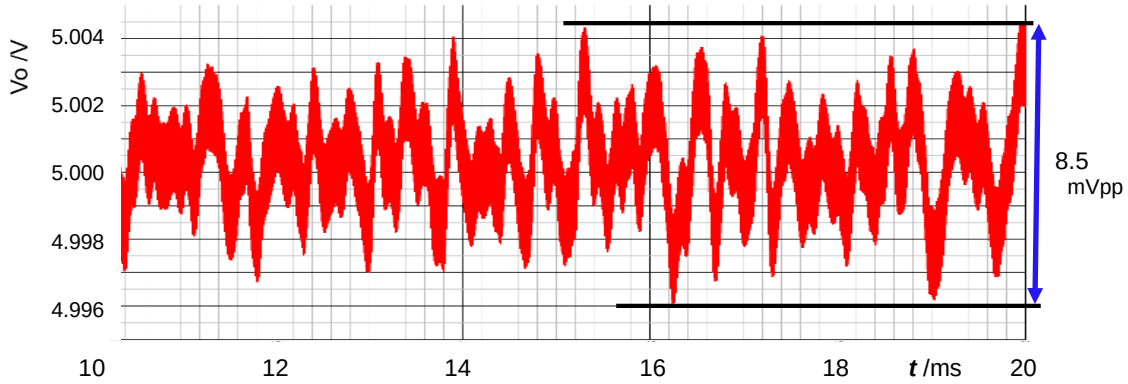


Fig. 18 Output ripple with bit-reverse.

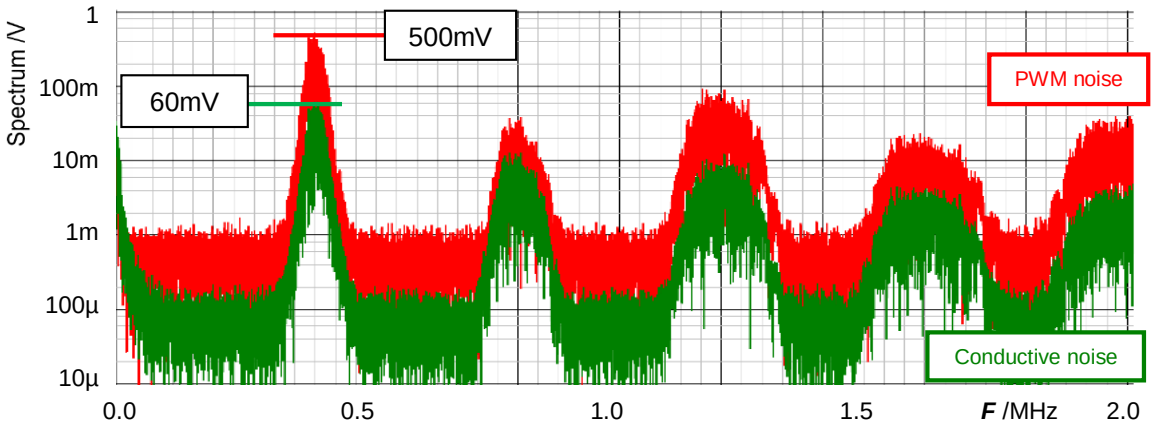


Fig. 19 Spectrum with bit-reverse.

4.3 Another analog pattern generator with bit exchange

In order to make the period of the analog noise much longer, we have utilized the bit-exchange shown below. In this case, there is no identical bit stream compared with Eq. (4-1) ~ (4-8) and the new pattern length of the analog noise becomes 6 times the original pattern, which is $T_2 = 6 \cdot T_1 = 96 \cdot To$.

	【Based on Eq. (3-1)】	【Based on Eq. (3-2)】	
1) $Q_1Q_2Q_3$:	0 - 1 - 3 - 6 - 5 - 2 - 4 -	: 0 - 1 - 2 - 5 - 3 - 6 - 4 -	(4-1)
2) $Q_1Q_3Q_2$:	0 - 1 - 5 - 6 - 3 - 4 - 2 -	: 0 - 1 - 2 - 5 - 3 - 6 - 4 -	(4-9)
3) $Q_2Q_1Q_3$:	0 - 2 - 3 - 5 - 6 - 1 - 4 -	: 0 - 1 - 2 - 5 - 3 - 6 - 4 -	(4-10)
4) $Q_2Q_3Q_1$:	0 - 4 - 5 - 3 - 6 - 1 - 2 -	: 0 - 1 - 2 - 5 - 3 - 6 - 4 -	(4-11)
5) $Q_3Q_1Q_2$:	0 - 2 - 6 - 5 - 3 - 4 - 1 -	: 0 - 1 - 2 - 5 - 3 - 6 - 4 -	(4-12)
6) $Q_3Q_2Q_1$:	0 - 4 - 6 - 3 - 5 - 2 - 1 -	: 0 - 1 - 2 - 5 - 3 - 6 - 4 -	(4-13)

4.4 New pattern generator and simulation results with bit-exchange

Fig. 20 shows the block diagram of the new M-sequence circuit with bit-exchange. Bit-exchanges are operated in the matrix block after the bit-reverse block. At the DAC output, there appear the analog steps of 48 times of the original pattern. Fig. 21 shows the new expanded bit pattern generated from the circuit in Fig. 20.

Fig. 22 shows the simulated spectrums using the new analog noise generator with bit-reverse and exchange. The peak level of the PWM pulse is 400 mV (-17.5 dB) and that of the conductive noise is 60mV which is equal level to the one in Fig. 19. The output ripple ⊿Vo is 8.5 mVpp as shown in Fig. 23 and the transient response is +- 22 mV as shown in Fig. 24 with the current step ⊿Io=0.25A, which is small enough because of less than 0.5% of the output voltage Vo=5.0V.

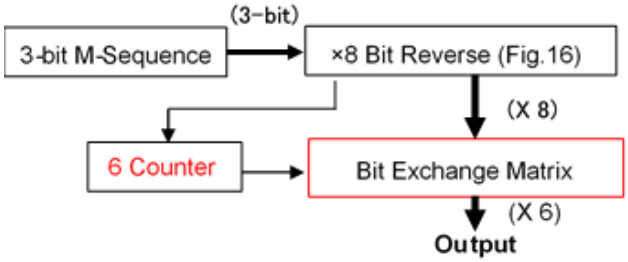


Fig. 20 Pattern generator with bit-exchange.

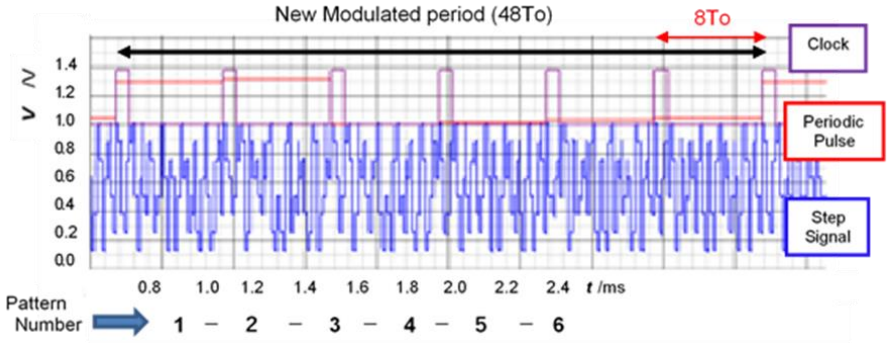


Fig. 21 Expanded pattern with bit-exchange.

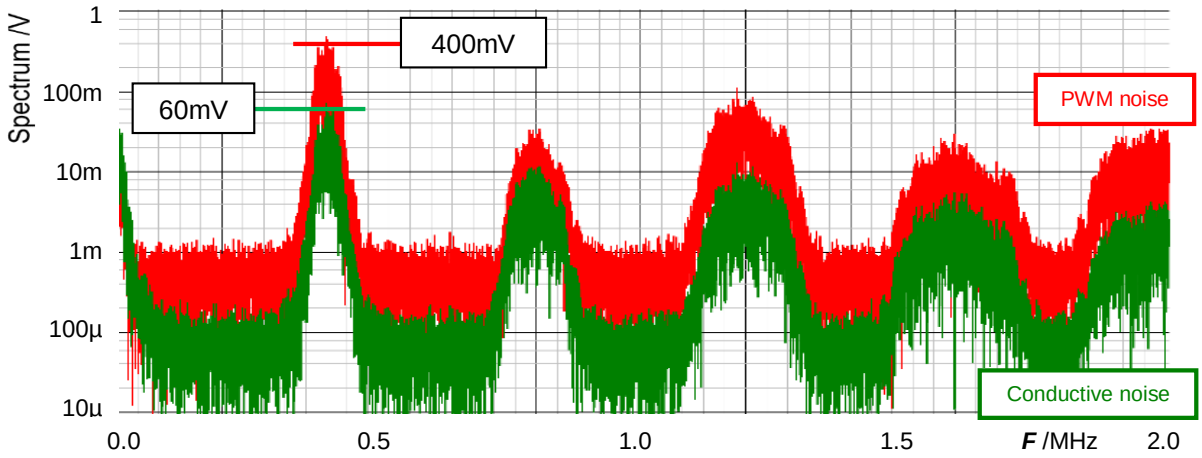


Fig. 22 Spectrum with bit-reverse & exchange.

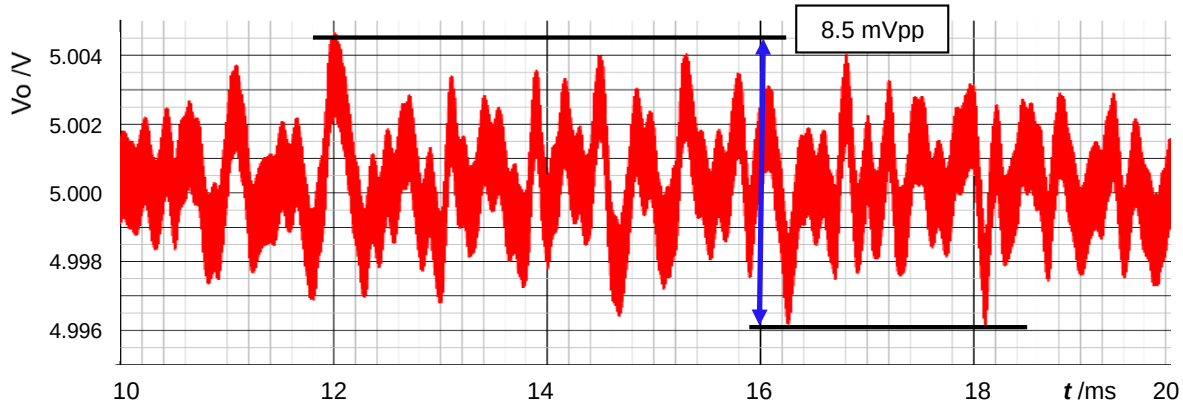


Fig. 23 Output ripple with bit-reverse & exchange.

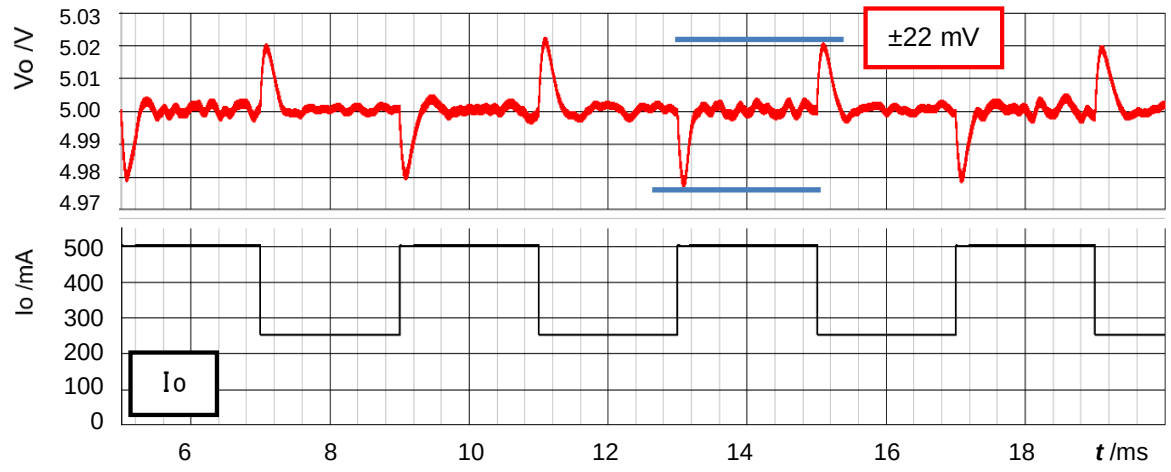


Fig. 24 Transient response with bit-reverse & exchange.

5. Bit Extension of Analog Noise Pattern Generator

5.1 Extension of bit number of pseudo analog noise generator

In the above explanation, the order of M-sequence bits in the primitive polynomial is 3. One might ponder that it is better for the reduction of the EMI noise to utilize the longer bit of the M-sequence circuit. However, in fact, what really reduces the EMI noise is not the order of the M-sequence circuit but the ratio of the variation of the pattern levels of the M-sequence generator.

Equations of 4th or 5th primitive polynomial are shown as below. There are 6 equations regarding the 5th-order primitive polynomial. The 4th-order primitive polynomials have two equations and the bit level series are shown in equations (5-9) (5-10). The number of the pattern variation is To=2^4−1=15.

[4th order] $G1(x)= x^4 + x^3 + 1$ (5-1)

$G2(x)= x^4 + x + 1$ (5-2)

[5th order] $G1(x)= x^5 + x^2 + 1$ (5-3)

$G2(x)= x^5 + x^3 + 1$ (5-4)

$G3(x)= x^5 + x^3 + x^2 + x + 1$ (5-5)

$G4(x)= x^5 + x^4 + x^2 + x + 1$ (5-6)

$G5(x)= x^5 + x^4 + x^3 + x + 1$ (5-7)

$G6(x)= x^5 + x^4 + x^3 + x^2 + 1$ (5-8)

[Pattern] G1：0-1-3-7-14-13-11-6-12-9-2-5-10-4-8- (5-9)

G2：0-1-2-5-10-4-9-3-6-13-11-7-14-12-8- (5-10)

5.2 Simulation results of analog noise generator with 4th order primitive polynomials

Fig. 25 shows the output step pattern from the 4th order M-sequence circuit and the output of the LPF with bit-reverse of Eq. (5-1) and (5-2). The step pattern is non-periodic pulses because each initial bit condition of the M-sequence generator is different, depending on the previous bit patterns.

Fig. 26 shows the spectrum of the PWM pulse. The peak level of the fundamental frequency is 600 mV, which is equal to that of the spectrum with 3rd order primitive polynomials. Fig. 27 shows the output ripple ⊿Vo of about 13mVpp.

There is no difference concerned with the EMI reduction of the spectrum between the 3rd and 4th M-sequence generators with bit reverse operation. It is enough to use only the 3-bit M-sequence circuit (3rd primitive polynomial). Its reason would be that the frequency modulation band is important, but not fine change of the frequency modulation, for the EMI reduction.

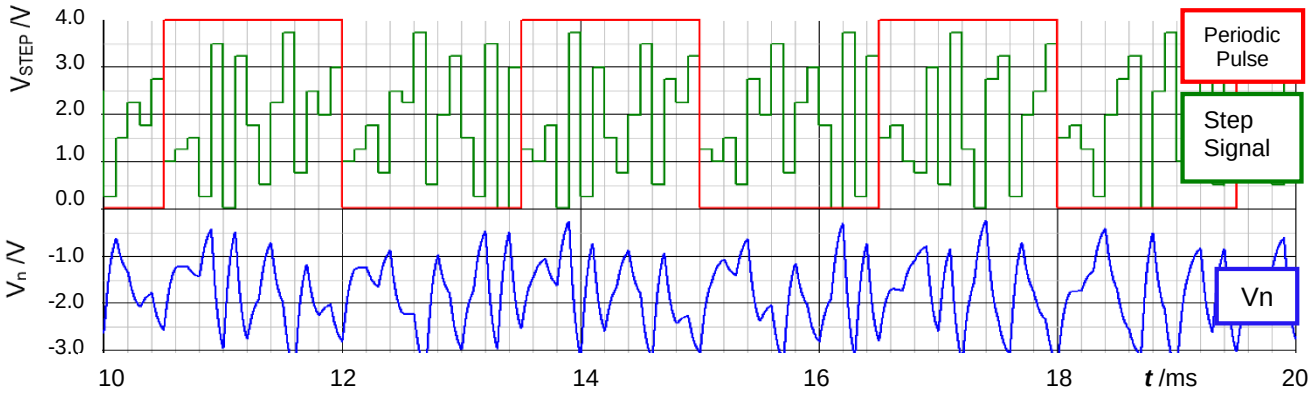


Fig. 25 Output signals from M-sequence generator of 4th order with bit-reverse.

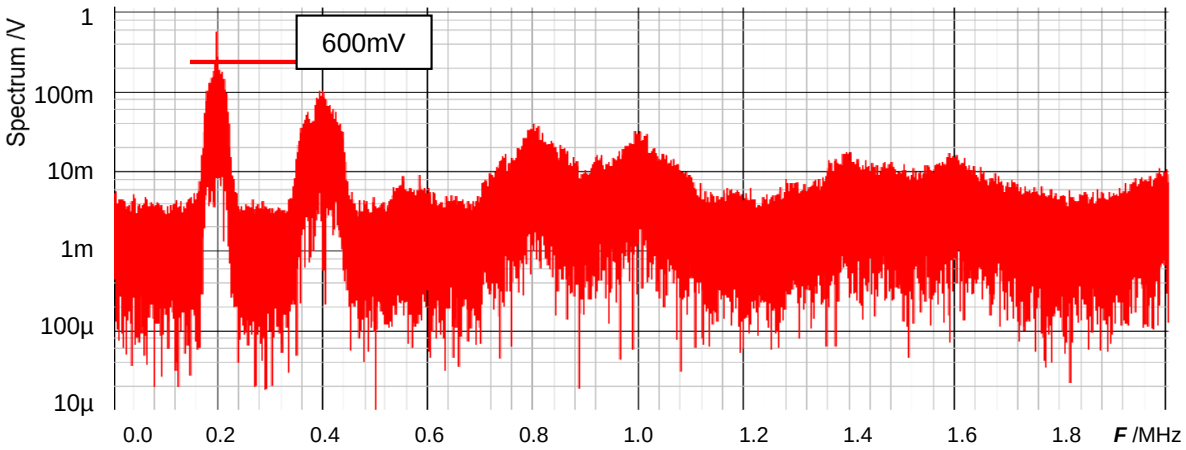


Fig. 26 Spectrum of PWM pulse with 4th order with bit-reverse.

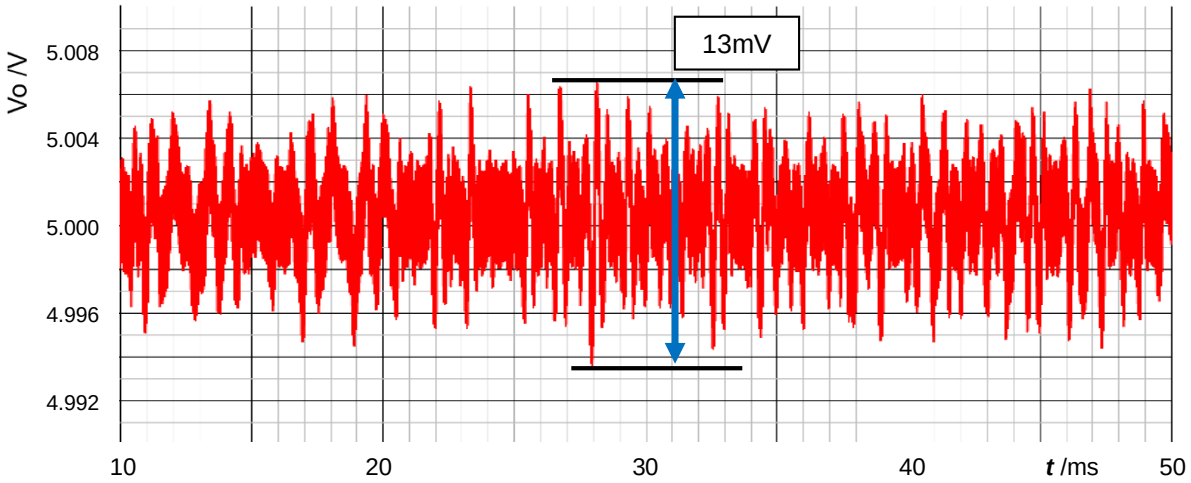


Fig. 27 Output ripple with 4th order.

5.3 Comparison with the Spread Spectrum Clock Generator (SSCG) method

There are other EMI noise reduction technologies [9] using the Spread Spectrum Clock Generator (SSCG) method, which utlize the frequency modulation technology for the PWM pulse by the sine wave, the triangular wave and so on. Fig. 28 shows the clock generator (Clock) which is shown in Fig. 1. It consists of the Voltage Controlled Osclator (VCO), which is controlled by the bias voltage (Vb) and the modulation signal (Vm). The output of the modified clock generator triggers the sawtooth (SAW) genarator.

Fig. 29 shows the simulation results of the clock modulated converter with the SSCG method. The peak level of the SAW signal changes synchlonizing with the triangular modulation signal. Note that the output voltage ripple is much increased synchrolized with the modulation signal ⊿Vo=20mV shown in Fig. 29. Here, Vo is the normal output ripple (about 3 mV) without modulation. The conditions of this SSCG converter: the modulation frequency is 1 kHz and the variation of the clock frequensy is 200kHz ±50kHz.

Fig. 30 shows the spectrum level of the PWM pulse of the SSCG method. The level of the clock frequency is 450 mV, which is 17dB reduction from the original level 3.2V. Here, the bottom figure shows the spectrum of the input current (Iin).

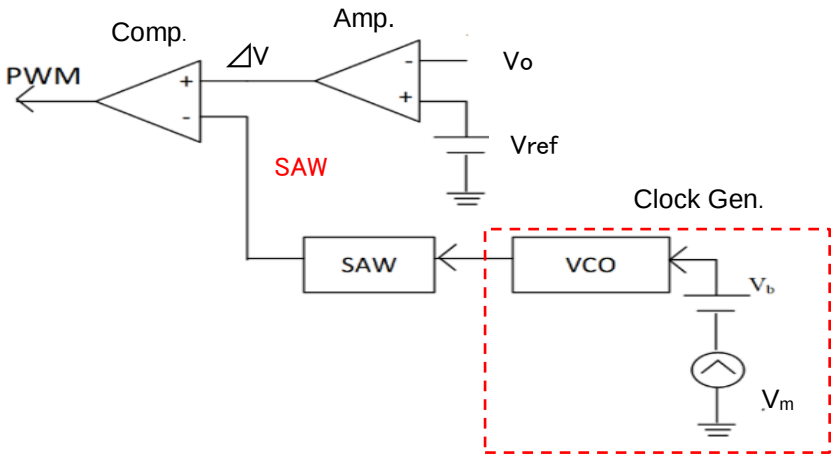


Fig. 28 Converter with SSCG method

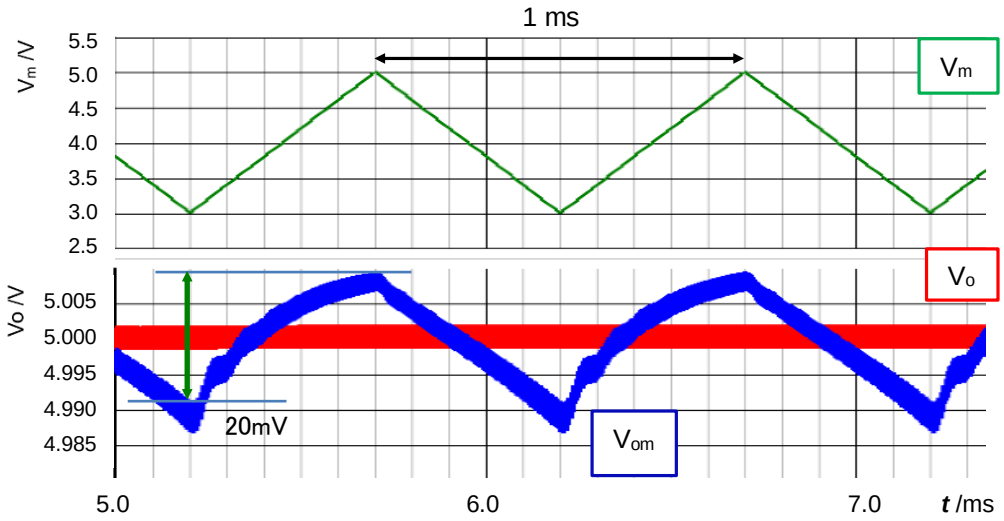


Fig. 29 Simulation results of SSCG converter

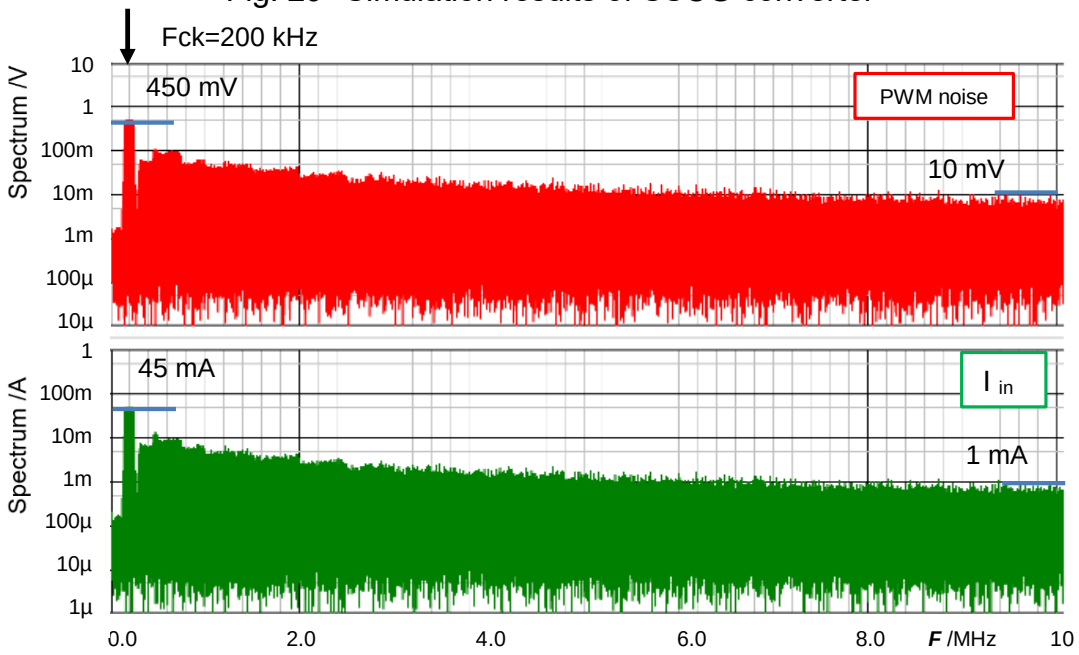


Fig. 30 Spread spectrum of SSCG converter

We compare the features of the proposed Pseudo Random Analog Noise (PRAN) method with those of this SSCG method.

1) Characteristics:

In the converter with the SSCG method, the spectrum level of the PWM frequency can be largely reduced by making the amplitude of the modulation signal large. However, its output voltage ripple goes up very large, which is no good for the voltage regulator. In the converter with the PRAN method, the output ripple stays almost the same as that without the clock modulation, which is only about 10mV shown in Fig. 21 and 25.

2) Cost and circuit (footprint) in case of integration:

They are almost the same because most of the circuits are digital and main components are the VCO in the SSCG method and the PLL circuit (which consists of the VCO and filter (capacitors)) in the PRAM method.

3) Complexity:

In the SSCG method, significant reduction of the EMI noise without the output ripple increase is difficult; so far how to design the modulation signal to suppress the output ripple is not clear. On the other hand, in the APAM method, the EMI noise level is largely reduced without the increase of the output ripple by designing the modulation pattern shown in Fig. 25, which is easily optimized by checking the output ripple waveform.

6. Conclusion

This paper proposes a new EMI reduction method by extended spread spectrum using the PLL circuit with pseudo analog noise which is produced from the M-sequence circuit. The PLL circuit makes the reference clock modified with non-periodic analog noise, which is supplied from the 3-bit M-sequence circuit with the 3rd order primitive polynomial. Extended pseudo analog noise is produced by reversing and/or exchanging the output bits from the M-sequence circuit. Using this modified clock, supplied from the PLL circuit for the saw-tooth signal in the switching converter, the spectrum of the PWM pulses is widely spread and the peak level of the spectrums of the fundamental frequency (400 kHz) and the harmonic frequencies are significantly reduced. The peak spectrum level at 400 kHz is reduced from 3.0V to 0.40V (17.5dB reduction) with bit-reverse and bit-exchange operations.

Notice that there is another reduction technology reported [9] which uses the linear sweep method. This method is easy to reduce the EMI noise; it modifies the clock frequency with the triangular signal. However, the output voltage ripple ΔVo increases in proportion to the EMI reduction level, and hence it is difficult to reduce the EMI noise substantially without the increase of the output ripple.

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